RTL8181/RTL8181P

WIRELESS LAN ACCESS POINT/ GATEWAY CONTROLLER

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2003/10/02	First release.
1.01	2003/12/12	1. Change CKVCO pin to 'Not used' on 208 (61, 62) and 292 (U19, U20, H17) in Table 10, page 12. 2. Add 'MA7' pin 143 on 208 to Table 1, page 5. 3. Add 'WTXEN' pin W13 to Table 12, page 15.

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1. Introduction

The RTL8181/RTL8181P is a highly integrated system-on-a-chip (SoC), embedded with a high-performance 32-bit RISC microcontroller, Ethernet, and WLAN controller. It is a cost-effective and high-performance solution for wireless LAN Access Point, wireless SOHO router, wireless Internet gateway systems, etc.

Two versions are available: The RTL8181 208-Pin QFP (Without PCI Interface), and the RTL8181P 292-Pin TFBGA, with a PCI interface for seamless connection of a PCI device. For example, an IEEE 802.11a device could be connected through this PCI interface to provide a WLAN dual mode service.

The embedded processor is a Lexra LX5280 32-bit RISC CPU, with separate 8K instruction and 8K data caches. A Memory Management Unit (MMU) allows the memory to be segmented and protected. Such protection is a requirement of modern operating systems (e.g., Windows NT, 2000, XP, Linux).

The processor pipeline is a dual-issue 6-stage architecture. The dual-issue CPU fetches two instructions per cycle, allowing two instructions to be executed concurrently in two pipes for an up to 30% improvement over uni-scalar architecture.

It includes two Fast Ethernet MACs, one possibly used for the LAN interface and the other connected to a WAN port. An IEEE 802.11b WLAN MAC+Baseband processor is embedded, saving costs and space compared with systems designed with an external 802.11b adapter.

The RTL8181/RTL8181P integrates a memory controller, providing a glueless interface to external SDRAM and Flash memory.

2. Features

Core Processor
- LX5280 32-bit RISC architecture.
- Superscalar architecture containing two execution pipelines for better performance.
- Embedded 8K I-Cache, 8K D-Cache, and 4K D-RAM.
- Memory Management Unit (MMU).
- Up to 200MHZ operating frequency.

WLAN Controller
- Integrated IEEE 802.11b compliant MAC and DSSS Baseband processor.
- Data rate of 11M, 5.5M, 2M, and 1M.
- Supports long and short preamble.
- Antenna diversity and Automatic Gain Control (AGC).
- Embedded encryption/decryption engine for 64-bit and 128-bit WEP.

Fast Ethernet Controller
- Fully compliant with IEEE 802.3/802.3u.
- Supports MII interface with full and half duplex capability.
- Supports descriptor-based buffer management with scatter-gather capability.
- Supports IP, TCP, and UDP checksum offload.
- Supports IEEE 802.1Q VLAN tagging and 802.1P priority queue.
- Supports full duplex flow control (IEEE 802.3X).

UART
- 16550 compatible.
- 16-byte FIFO buffer size.
- Auto CTS/RTS flow control.

Memory Controller
- Supports external 16/32-bit SDRAM with 2-bank access, up to 32Mbytes.
- Supports external 16-bit Flash memory, up to 16Mbytes.

PCI Bridge (RTL8181P Only)
- Complies with PCI 2.2.
- Supports two external PCI devices.
- Supports PCI master/slave mode.
- 3.3 and 5V I/O tolerance.

GPIO
- 16 programmable I/O ports (plus additional 16 ports when memory interface in 16-bit mode).
- Individually configurable as input, output, and edge transition.

Watchdog/Timer/Counter
- Hardware watchdog timer, used to reset the processor if the system hangs.
- Four sets of general timers/counters.

EJTAG
- Standard P1149.1 JTAG interface for testing and debugging.

Package
- RTL8181 208-Pin QFP (Without PCI Interface).
- RTL8181P 292-Pin TFBGA (With PCI Interface).

3. Block Diagram

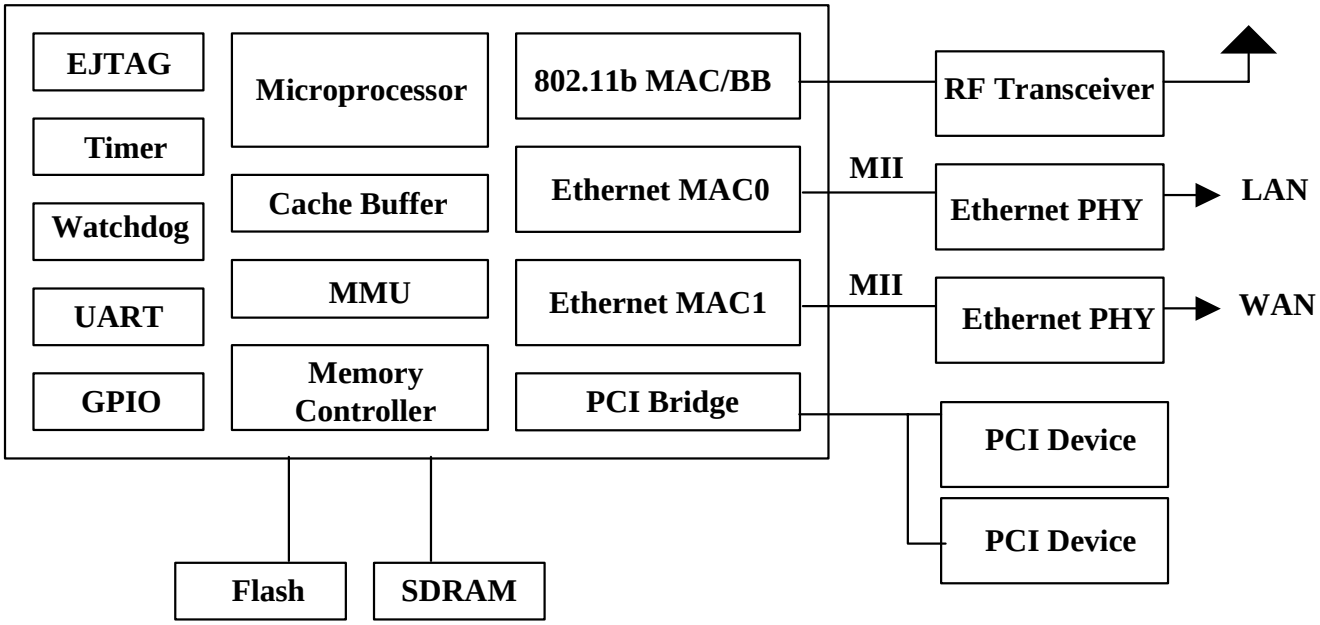


Figure 1. Block Diagram

4. Pin Assignments

4.1. RTL8181P Pin Assignments

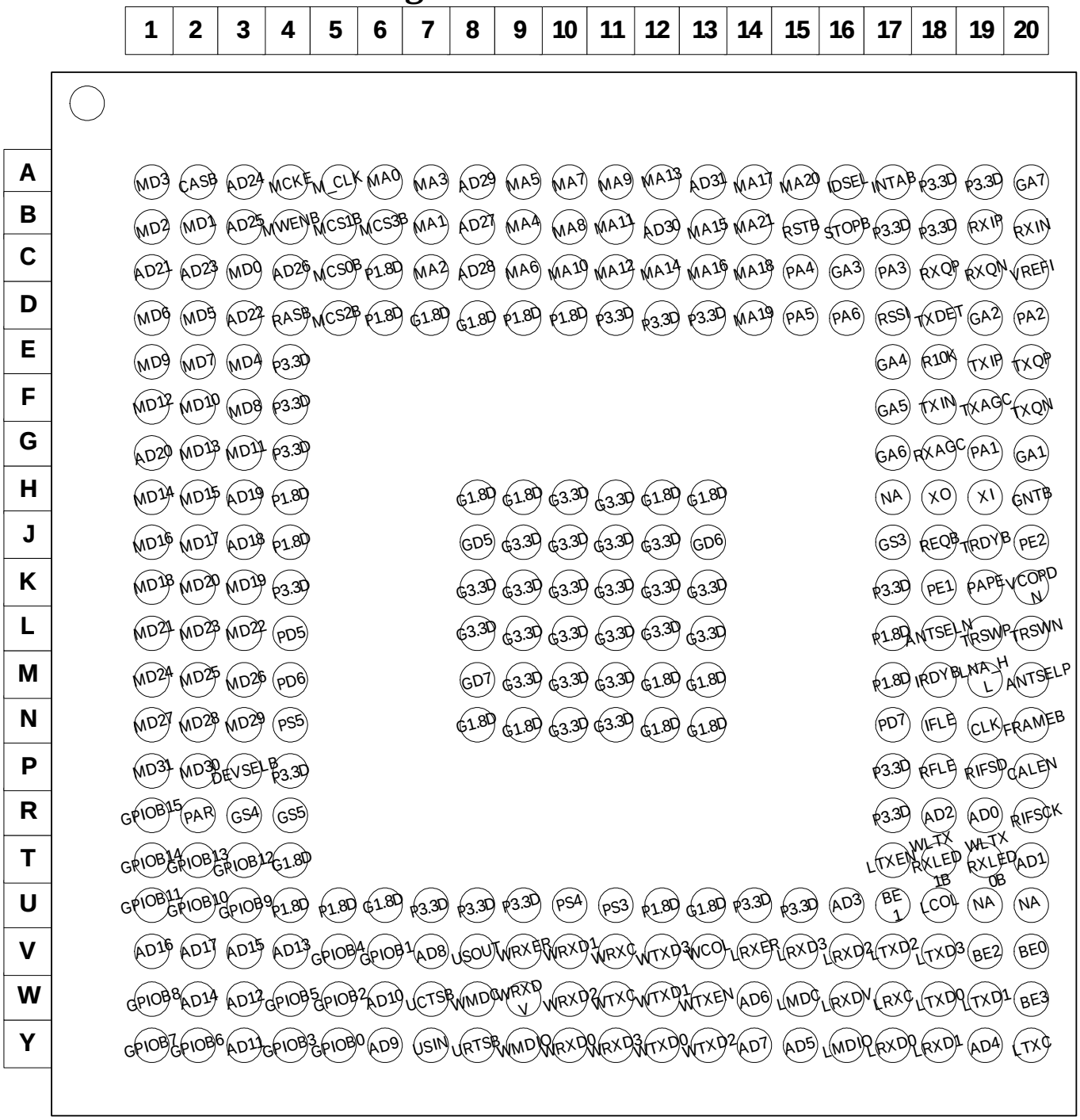


Figure 2. RTL8181P 292-Pin TFBGA Pin Assignments

4.2. RTL8181 Pin Assignments

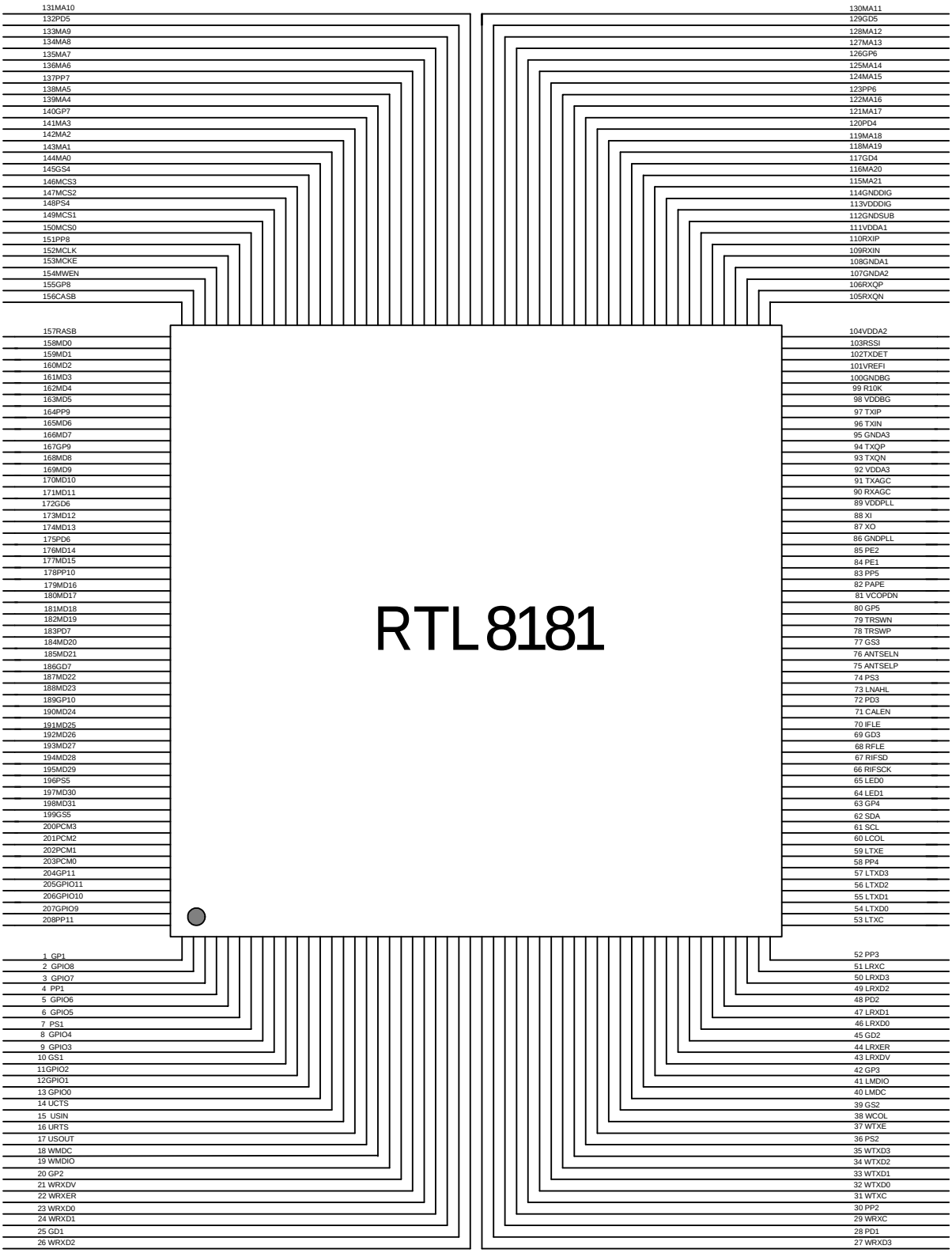


Figure 3. RTL8181 208-Pin QFP Pin Assignments

5. Pin Descriptions

5.1. Memory Interface

Table 1. Memory Interface

Symbol	Type	Pin No (208)	Pin No (292)	Description
MD[31-0]	I/O	198, 197, 195, 194, 193, 192, 191, 190, 188, 187, 185, 184, 182, 181, 180, 179, 177, 176, 174, 173, 171, 170, 169, 168, 166, 165, 163, 162, 161, 160, 159, 158	P1, P2, N3, N2, N1, M3, M2, M1, L2, L3, L1, K2, K3, K1, J2, J1, H2, H1, G2, F1, G3, F2, E1, F3, E2, D1, D2, E3, A1, B1, B2, C3	Data for SDRAM, Flash.
MA[21-0]/ DQM[3-0]	O	115, 116, 118, 119, 121, 122, 124, 125, 127, 128, 130, 131, 133, 134, 135, 136, 138, 139, 141, 142, 143, 144	B14, A15, D14, C14, A14, C13, B13, C12, A12, C11, B11, C10, A11, B10, A10, C9, A9, B9, A7, C7, B7, A6	Address for SDRAM, Flash. MA[15-18] mapping to DQM[3-0] for SDRAM.
M_CLK	O	152	A5	SDRAM clock.
MCS0B	O	150	C5	Bank 0 chip select, FLASH chip select.
MCS1B	O	149	B5,	Bank 1 chip select, FLASH chip select.
RASB/OEB	O	157	D4	Raw address strobe for SDRAM; Output enable for Flash.
CASB	O	156	A2	Column address strobe.
MWENB	O	154	B4	Write enable for SDRAM and Flash.
MCKE	O	153	A4	SDRAM Clock enable.
MCS2B	O	147	D5	Bank 0 chip select for SDRAM.
MCS3B	O	146	B6	Bank 1 chip select for SDRAM.

5.2. UART Interface

Table 2. UART Interface

Symbol	Type	Pin No (208)	Pin No (292)	Description
URTSB	O	16	Y8	UART Request to send.
UCTSB	I	14	W7	UART Clear to send.
USIN	I	15	Y7	UART data receive serial input.
USOUT	O	17	V8	UART data transmit serial output.

5.3. Power & GND

Table 3. Power & GND

Symbol	Type	Pin No (208)	Pin No (292)	Description
P3.3D	P	208, 178, 164, 151, 137, 123, 83, 58, 52, 30, 4	K4, G4, F4, E4, D13, D12, D11, B18, B17, A19, A18, K17, P4, P17, R17, U7, U8, U14, U9, U15	I/O power 3.3V (Digital).
G3.3D	P	204, 189, 167, 155, 140, 126, 80, 63, 42, 20, 1	K12, K11, K10, K9, K8, J12, J11, J10, J9, H11, H10, K13, L8, L9, L10, L11, L12, L13, M9, M10, M11, N10, N11	I/O 3.3V GND (Digital).
PD[7:5],PS[5:3]	P	183, 175, 132, 196, 148, 74	N17, M4, L4, N4, U10, U11	Core logic power 1.8V (Digital).
GD[7-5], GS[5-3]	P	186, 172, 129, 199, 145, 77	M8, J13, J8, R4, R3, J17	Core logic 1.8 Ground (Digital).
PA[6-1]	P	111, 104, 92, 113, 98, 89	D16, D15, C15, C17, D20, G19	Wireless LAN Power 3.3V(Analog).
GA[6-1], GA7	P	108, 107, 95, 114, 100, 86, 112	G17, F17, E17, C16, D19, G20, A20	Wireless LAN Ground (Analog), GA7 VSUB.
P1.8D	P	120, 72, 48, 28, 36, 7	J4, H4, D10, D9, D6, C6, U4, U5, U12, L17, M17	Core logic 1.8V Power (Digital).
G1.8D	P	117, 69, 45, 25, 39, 10	H13, H12, H9, H8, M12, M13, N8, N9, N12, N13, D8, D7, T4, U6, U13	Core logic Ground (Digital).

5.4. WLAN Traffic LED Control

Table 4. WLAN Traffic LED Control

Symbol	Type	Pin No (208)	Pin No (292)	Description
WLTXRXLED0B	O	65	T19	WLAN Tx/Rx traffic indicator or JTAG reset.
WLTXRXLED1B	O	64	T18	WLAN Tx/Rx traffic indicator or JTAG CLK.

5.5. RF Interface for Intersil

Table 5. RF Interface for Intersil

Symbol	Type	Pin No (208)	Pin No (292)	Description
RIFSCK	O	66	R20	3-wire Bus Clock.
RIFSD	O	67	P19	3-wire Bus Data.
RFLE	O	68	P18	3-wire Bus Enable.
IFLE/AGCSET	O	70	N18	IF_LE of the Intersil Chipset: PLL Synthesizer Serial Interface Latch Enable Control. CMOS output.
CALEN/ AGCRESET	O	71	P20	CAL_EN of the Intersil Chipset: CMOS output for activation of DC offset adjust circuit. A rising edge activates the calibration cycle, which completes within a programmable time and holds the calibration while this pin is held high. In applications where the synthesizer is not used, this pin needs to be grounded.

Symbol	Type	Pin No (208)	Pin No (292)	Description
LNA_HL	O	73	M19	Drive to the RF AGC Stage Attenuator: CMOS digital.
ANTSELP/ ANTSELN	O O	75 76	M20 L18	Antenna Select Pin. 10: Select Antenna A 01: Select Antenna B
TRSWP TRSWN	O O	78 79	L19 L20	Transmit/Receive Control.
VCOPDN/ PHITXI	O	81	K20	Output Pin as VCO VCC Power Enable/Disable.
PAPE	O	82	K19	Transmit PA Power Enable.
PE1/PHITXQ	O	84	K18	The combinations of PE1 and PE2 are as follows: 00: Power Down State, PLL Registers in Save Mode, Inactive PLL, Active Serial 11: Receive State, Active PLL 10: Transmit State, Active PLL 01: Inactive Transmit and Receive States, Active PLL, Active Serial Interface
PE2	O	85	J20	Output Pin as PE2: Refer to PE1 description.
RXIP RXIN	**AI AI	110 109	B19 B20	Receive (Rx) In-phase Differential Analog Data.
RXQP RXQN	AI AI	106	C18, C19	Receive (Rx) Quadrature Differential Analog Data.
RSSI	AI	105	D17	Analog Input to the Receive Power A/D Converter for AGC Control.
TXDET	AI	102	D18	Input to the Transmit Power A/D Converter for Transmit AGC Control.
VREFI	AI	101	C20	Voltage Reference for ADC and DAC.
TXIP TXIN	AO AO	97 96	E19, F18	Transmit (Tx) In-phase Differential Analog Data.
TXQP TXQN	AO AO	94 93	E20, F20	Transmit (Tx) Quadrature Differential Analog Data.
TXAGC	AO	91	F19	Analog Drive to the Transmit IF Power Control.
RXAGC	AO	90	G18	Analog Drive to the Receive IF AGC Control.

***A=Analog Signal*

5.6. RF Interface for RFMD

Table 6. RF Interface for RFMD

Symbol	Type	Pin No (208)	Pin No (292)	Description
RIFSCK	O	66	R20	3-wire Bus Clock: Serial clock output, with resistive dividers on board to allow programming from +5V levels.
RIFSD	O	67	P19	3-wire Bus Data: Serial data output, with resistive dividers on board to allow programming from +5V levels.
RFLE	O	68	P18	3-wire Bus Enable: Enable serial port output, with resistive dividers on board to allow programming from +5V levels.
IFLE/AGCSET	X	70	N18	Not used in the RFMD RF chipset.
CALEN/ AGCRESET	X	71	P20	Not used in the RFMD RF chipset.
LNA_HL	O	73	M19	RF2494 Gain Select: Digital output.

Symbol	Type	Pin No (208)	Pin No (292)	Description
ANTSELP	O	75	M20	Antenna Select Pin. 10: Select Antenna A 01: Select Antenna B
ANTSELN	*X	76	L18	Not used in the RFMD RF chipset.
TRSWP	X	78	L19	Not used in the RFMD RF chipset.
TRSWN	X	79	L20	Not used in the RFMD RF chipset.
VCOPDN/ PHITXI	O/I	81	K20	Output Pin as VCO VCC Power Enable/Disable.
PAPE	O	82	K19	Power Control Output for RF2189 PA: 0V to +3.3V.
PE1/PHITXQ	O	84	K18	This pin is the shutdown control output on board regulator when the RF Module enters either power-saving or standby mode.
PE2	O	85	J20	Output pin as RF2948 RX EN/ TX EN, RF2494 OE and CE: Refer to the RF2948 and RF2494 datasheets.
RXIP	**AI	110	B19	Receive (Rx) In-phase Analog Data in Single Ended
RXIN	X	109	B20	Not used in RFMD RF chipset.
RXQP	AI	106	C18	Receive (Rx) Quadrature-phase Analog Data in Single Ended
RXQN	X	105	C19	Not used in RFMD RF chipset.
RSSI	X	103	D17	Not used in RFMD RF chipset.
TXDET	AI	102	D18	To internal ADC, which detects transmit power.
VREFI	AI	101	C20	Reference voltage for ADC, DAC from VREF1 of RF2948B.
TXIP	AO	97	E19	Transmit (Tx) In-phase Digital Data: Combine before connecting to TX_I of RF2948B.
TXIN	AO	96	F18	
TXQP	AO	94	E20	Transmit (Tx) Quadrature Digital Data: Combine before connecting to TX_Q of RF2948B.
TXQN	AO	93	F20	
TXAGC	AO	91	F19	Transmit gain control output to RF2948.
RXAGC	AO	90	G18	RF2948 VGC receiver gain control analog output.

**X=Not used*
***A=Analog signal*

5.7. RF Interface for Philips

Table 7. RF Interface for Philips

Symbol	Type	Pin No (208)	Pin No (292)	Description
RIFSCK	O	66	R20	3-wire Bus Clock: RIFSCK is the ‘shift clock’ output. If the 3-wire bus is enabled, address or data bits will be clocked out from the RIFSD pin on rising edges of RIFSCK.
RIFSD	O	67	P19	3-wire Bus Data: RIFSD is the output “data” pin.
RFLE	O	68	P18	3-wire Bus Enable: RFLE is an “enable” signal. It is level sensitive: If RFLE is of LOW value, the 3-wire bus interface on the SA2400 is enabled. This means that each rising edge on the RIFSCK pin is taken as a shift cycle, and address/data bits are expected on RIFSD. If RFLE is HIGH, the 3-wire bus interface is disabled. No register settings will change regardless of activity on RIFSCK and RIFSD.

Symbol	Type	Pin No (208)	Pin No (292)	Description
IFLE/AGCSET	I	70	N18	AGCSET of the Philips Chipset: On the digital output pin AGCRESET, a 0 => 1 transition clears AGCSET of SA2400 to logic 0 and SA2400 starts the AGC cycle. At end of the AGC cycle, the AGCSET of SA2400 is asserted to logic 1. Then, AGCRESET will return to logic low.
CALEN/ AGCRESET	O	71	P20	AGCRESET of the Philips Chipset: Please refer to the AGCSET description and Philips SA2400 datasheet.
LNA_HL	*X	73	M19	Not used in Philips RF chipset.
ANTSELP/ ANTSELN	O O	75 76	M20 L18	Antenna Select Pin. 10: Select Antenna A 01: Select Antenna B
TRSWP	O	78	L19	Transmit and Receive Switch Control: This is a complement for TRSW-. 0: RX 1: TX
TRSWN	O	79	L20	Transmit and Receive Switch Control: This is a complement for TRSW+. 0: TX 1: RX
VCOPDN/ PHITXI/	O/I	81	K20	Output Pin as Transmit (Tx) In-phase Digital Data of the Philips Chipset. This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
PAPE	O	82	K19	Transmit PA Power Enable: Assert high when starting transmission.
PE1/PHITXQ	O	84	K18	Transmit (Tx) Quadrature Digital Data of Philips Chipset. This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
PE2	O	85	J20	Output Pin as TX/RX Control: 0: TX 1: RX
RXIP	**AI	110	B19	Receive (Rx) In-phase Analog Data: Positive path of differential pair.
RXIN	AI	109	B20	Receive (Rx) In-phase Analog Data: Negative path of differential pair.
RXQP	AI	106	C18	Receive (Rx) Quadrature-phase Analog Data. Positive path of the differential pair.
RXQN	AI	105	C19	Receive (Rx) Quadrature-phase Analog Data. Negative path of the differential pair.
RSSI	AI	103	D17	Received Signal Strength Indication. To internal ADC.
TXDET	AI	102	D18	Transmit Power Detect. To internal ADC, which detects transmit power.
VREFI	AI	101	C20	Reference Voltage for ADC & DAC
TXIP	AO	97	E19	Transmit (Tx) In-phase Analog Data. Positive path of differential pair. This function is valid in Tx digital mode (AnalogPhy = Digital on EEPROM writer program).

Symbol	Type	Pin No (208)	Pin No (292)	Description
TXIN	AO	96	F18	Transmit (Tx) In-phase Analog Data. Negative path of differential pair. This function is valid in Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXQP	AO	94	E20	Transmit (Tx) Quadrature-phase Analog Data. Positive path of the differential pair. This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXQN	AO	93	F20	Transmit (Tx) Quadrature-phase Analog Data. Negative path of the differential pair. This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXAGC	X	91	F19	Not used in the Philips RF chipset.
RXAGC	X	90	G18	Not used in the Philips RF chipset.

**X=Not used*
***A=Analog signal*

5.8. RF Interface for Maxim

Table 8. RF Interface for Maxim

Symbol	Type	Pin No (208)	Pin No (292)	Description
RIFSCK	O	66	R20	3-wire Bus Clock: Serial clock output.
RIFSD	O	67	P19	3-wire Bus Data: Serial data output.
RFLE	O	68	P18	3-wire Bus Enable: Enable serial port output.
IFLE/AGCSET	*X	70	N18	Not used in the Maxim RF chipset.
CALEN/ AGCRESET	X	71	P20	Not used in the Maxim RF chipset.
LNA_HL	O	73	M19	LNA Gain Select Logic Output: Logic high for LNA high-gain mode, logic low for LNA low-gain mode.
ANTSELP	O	75	M20	Antenna Select Pin. 10: Select Antenna A 01: Select Antenna B
ANTSELN	X	76	L18	Not used in the Maxim RF chipset.
TRSWP	X	78	L19	Not used in the Maxim RF chipset.
TRSWN	X	79	L20	Not used in the Maxim RF chipset.
VCOPDN/ PHITXI	O/I	81	K20	Output Pin as VCO VCC Power Enable/Disable.
PAPE	O	82	K19	Transmit PA Power Enable. Assert high when starting transmission.
PE1/PHITXQ	O	84	K18	Not used in the Maxim RF chipset.
PE2	O	85	J20	Not used in the Maxim RF chipset.
RXIP	**AI	110	B19	Receive (Rx) In-phase Analog Data. Positive path of differential pair.
RXIN	X	109	B20	Receive (Rx) In-phase Analog Data. Negative path of differential pair.
RXQP	AI	106	C18	Receive (Rx) Quadrature-phase Analog Data. Positive path of differential pair.
RXQN	X	105	C19	Receive (Rx) Quadrature-phase Analog Data. Negative path of differential pair.
RSSI	X	103	D17	Not used in the Maxim RF chipset.
TXDET	AI	102	D18	To internal ADC, which detects transmit power.

Symbol	Type	Pin No (208)	Pin No (292)	Description
VREFI	AI	101	C20	Not used in the Maxim RF chipset.
TXIP	AO	97	E19	Transmit (Tx) In-phase Digital Data. Combine before connecting to TX_I of RF2948B.
TXIN	AO	96	F18	
TXQP	AO	94	E20	Transmit (Tx) Quadrature Digital Data. Combine before connecting to TX_Q of RF2948B.
TXQN	AO	93	F20	
TXAGC	AO	91	F19	Transmit gain control output to RF2948.
RXAGC	AO	90	G18	Analog Drive to the Receiver AGC Control.

**X=Not used*
***A=Analog signal*

5.9. RF Interface for GCT

Table 9. RF Interface for GCT

Symbol	Type	Pin No (208)	Pin No (292)	Description
RIFSCK	O	66	R20	3-wire Bus Clock. RIFSCK is the 'shift clock' output. If the 3-wire bus is enabled, address or data bits will be clocked out from the RIFSD pin on rising edges of RIFSCK.
RIFSD	O	67	P19	3-wire Bus Data: Serial data output.
RFLE	O	68	P18	3-wire Bus Enable. RFLE is an 'enable' signal. It is level sensitive. If RFLE is of LOW value, the 3-wire bus interface on the GRF5101 is enabled. This means that each rising edge on the RIFSCK pin is taken as a shift cycle, and address/data bits are expected on RIFSD. If RFLE is HIGH, the 3-wire bus interface is disabled. No register settings will change regardless of activity on RIFSCK and RIFSD.
IFLE/AGCSET	*X	70	N18	Not used in the GCT RF chipset.
CALEN/ AGCRESET	X	71	P20	Not used in the GCT RF chipset.
LNA_HL	O	73	M19	GRF5101 Gain Select: Digital output.
ANTSELP/ ANTSELN	O O	75 76	M20 L18	Antenna Select Pin. 10: Select Antenna A 01: Select Antenna B
TRSWP	O	78	L19	Transmit and Receive Switch Control. This is a complement for TRSWN. 0:RX 1:TX
TRSWN	O	79	L20	Transmit and Receive Switch Control. This is a complement for TRSWP. 0:TX 1:RX
VCOPDN/ PHITXI	O/I	81	K20	Output Pin as VCO VCC Power Enable/Disable.
PAPE	O	82	K19	Transmit PA Power Enable. Assert high when starting transmission.
PE1/PHITXQ	O	84	K18	Transmit (Tx) Quadrature Digital Data of RF Chipset. This function is valid in Tx digital mode (AnalogPhy = Digital on EEPROM writer program).

Symbol	Type	Pin No (208)	Pin No (292)	Description
PE2	O/I	85	J20	Output Pin as TX/RX Control. 0:TX 1:RX
RXIP	**AI	110	B19	Receive (Rx) In-phase Analog Data. Positive path of differential pair.
RXIN	X	109	B20	Receive (Rx) In-phase Analog Data. Negative path of differential pair.
RXQP	AI	106	C18	Receive (Rx) Quadrature-phase Analog Data. Positive path of differential pair.
RXQN	X	105	C19	Receive (Rx) Quadrature-phase Analog Data. Negative path of differential pair.
RSSI	X	103	D17	Not used in the GCT RF chipset.
TXDET	AI	102	D18	To internal ADC, which detects transmit power.
VREFI	AI	101	C20	Reference Voltage for ADC & DAC.
TXIP	AO	97	E19	Transmit (Tx) In-phase Analog Data. Positive path of differential pair. This function is valid in Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXIN	AO	96	F18	Transmit (Tx) In-phase Analog Data. Negative path of differential pair. This function is valid in Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXQP	AO	94	E20	Transmit (Tx) Quadrature-phase Analog Data. Positive path of the differential pair. This function is valid in Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXQN	AO	93	F20	Transmit (Tx) Quadrature-phase Analog Data. Negative path of the differential pair. This function is valid in Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXAGC	X	91	F19	Not used in the GCT RF chipset.
RXAGC	AO	90	G18	GRF5101 VGC receiver gain control analog output.

**X=Not used*
***A=Analog signal*

5.10. Miscellaneous

Table 10. Miscellaneous

Symbol	Type	Pin No (208)	Pin No (292)	Description
R10K	I/O	99	E18	This pin must be pulled low by a 10K Ω resistor.
XO	O	87	H18	Crystal Feedback Output. This output is reserved for a crystal connection. It should be left open when XI is driven with an external 44 MHz oscillator.
XI	I	88	H19	44MHz OSC Input.
Not used	X	61, 62	U19, U20, H17	Not used. Must be open.

5.11. PCI Interface (RTL8181P Only)

The following signal type definitions are from the point of devices other than the arbiter.

IN: Input.

O: Output.

T/S: Tri-State bi-directional input/output pin.

S/T/S: Sustained Tri-State.

O/D: Open Drain.

Table 11. PCI Interface

Symbol	Type	Pin No (208)	Pin No (292)	Description
AD31-0	T/S	*X	A13, B12, A8, C8, B8, C4, B3, A3, C2, D3, C1, G1, H3, J3, V2, V1, V3, W2, V4, W3, Y3, W6, Y6, V7, Y14, W14, Y15, Y19, U16, R18, T20, R19	PCI address and data multiplexed pins. The address phase is the first clock cycle in which FRAMEB is asserted. During the address phase, AD31-0 contains a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a double-word address. Write data is stable and valid when IRDYB is asserted. Read data is stable and valid when TRDYB is asserted. Data I is transferred during those clocks where both IRDYB and TRDYB are asserted.
C/BE3-0	T/S	X	W20, V19, U17, V20	PCI bus command and byte enables multiplexed pins. During the address phase of a transaction, C/BE3-0 defines the bus command. During the data phase, C/BE3-0 are used as Byte Enables. Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0 applies to byte0, and C/BE3 applies to byte3.
CLK	IN	X	N19	PCI clock. This clock input provides timing for all PCI transactions and is input to the PCI device.
DEVSELB	S/T/S	X	P3	Device Select. As a bus master, the RTL8181P samples this signal to ensure that a PCI target recognizes the destination address for the data transfer.
FRAMEB	S/T/S	X	N20	Cycle Frame. As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is deasserted, the transaction is in the final data phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
GNTB	T/S	X	H20	Grant. Indicates to the agent that access to the bus has been granted.
REQB	T/S	X	J18	Request. Indicates to the arbiter that this agent desires use of the bus.
IDSEL	O	X	A16	Initialization Device Select. This pin is used as a chip select during configuration read and write transactions.

Symbol	Type	Pin No (208)	Pin No (292)	Description
INTAB	O/D	X	A17	Interrupt A. Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask.
IRDYB	S/T/S	X	M18	Initiator Ready. This indicates the initiating agent's ability to complete the current data phase of the transaction. As a bus master, this signal is asserted low when the RTL8181P is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus.
TRDYB	S/T/S	X	J19	Target Ready. This indicates the target agent's ability to complete the current phase of the transaction. As a bus master, this signal indicates that the target is ready for the data during write operations and holds the data during read operations. As a target, this signal is asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low.
PAR	T/S	X	R2	Parity. This signal indicates even parity across AD31-0 and C/BE3-0 including the PAR pin. PAR is stable and valid one clock after each address phase. For the data phase, PAR is stable and valid one clock after either IRDYB is asserted on a write transaction, or TRDYB is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. As a bus master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
STOPB	S/T/S	X	B16	Stop. Indicates that the current target is requesting the master to stop the current transaction.
RSTB	IN	X	B15	Reset. Active low signal to reset the PCI device.
REQ1B	T/S	X	R1	Request Indicates to the arbiter that this agent desires use of the bus.(The second PCI slot)
GNT1B	T/S	X	T1	Grant. Indicates to the agent that access to the bus has been granted. (The second PCI slot)
IDSEL1B	IN	X	T2	Initialization Device Select. This pin is used as a chip select during configuration read and write transactions. (The second PCI slot)

**X=Not used*

5.12. MII Interface

Table 12. MII Interface

Symbol	Type	Pin No (208)	Pin No (292)	Description
LTXC, WTXC	I	53, 31	Y20, W11	TXC is a continuous clock that provides a timing reference for the transfer of TXD[3:0], TXE. In MII mode, it uses the 25MHz or 2.5MHz supplied by the external PMD device.
LTXEN, WTXEN	O	59, 37	T17, W13	Indicates the presence of valid nibble data on TXD[3:0].
LTXD[3-0], WTXD [3-0]	O	57, 56, 55, 54 35, 34, 33, 32	V18, V17, W19, W18, V12, Y13, W12, Y12	Four parallel transmit data lines that are driven synchronous to the TXC for transmission by the external physical layer chip.
LRXC, WRXC	I	51, 29	W17, V11	This is a continuous clock that is recovered from the incoming data. MRXC is 25MHz in 100Mbps and 2.5Mhz in 10Mbps.
LCOL, WCOL	I	60, 38	U18, V13	This signal is asserted high synchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
LRXDV, WRXDV	I	43, 44	W16, W9	Data valid is asserted by an external PHY when receive data is present on the RXD[3:0] lines, and it is deasserted at the end of the packet. This signal is valid on the rising edge of the RXC.
LRXD[3-0], WRXD[3-0]	I	50, 49, 47, 46 27, 26, 24, 23	V15, V16, Y18, Y17, Y11, W10, V10, Y10	This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RXC by the external physical unit
LRXER, WRXER	I	44, 22	V14, V9	This pin is asserted to indicate that an invalid symbol has been detected in 100Mbps MII mode. This signal is synchronized to RXC and can be asserted for a minimum of one receive clock.
LMDC, WMDC	O	40, 18	W15, W8	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks.
LMDIO, WMDIO	I/O	41, 19	Y16, Y9	Management Data Input/Output. This pin provides a bi-directional signal used to transfer management information.

5.13. GPIO

Table 13. GPIO

Symbol	Type	Pin No (208)	Pin No (292)	Description
GPIOB[11-0]	I/O	205, 206, 207, 2, 3, 5, 6, 8, 9, 11, 12, 13	U1, U2, U3, W1, Y1, Y2, W4, V5, Y4, W5, V6, Y5	General Purpose I/O pins group B, pins 11 to 0. If ICFG[5-4] power on latch =[1-0]. GPIO[5-2] mapping to JTAG_TDO (JTAG test data output), JTAG_TRSTN(JTAG reset), JTAG_TMS (JTAG test mode select), JTAG_TDI (JTAG test data input).
GPIOB[15-12]	I/O	200, 201, 202, 203	R1, T1, T2, T3	General Purpose I/O pins group B, pin 15 to 12.

6. Address Mapping

The RTL8181/RTL8181P supports up to 4 gigabytes of address space. The memory map is managed by an MMU (Memory Management Unit) that translates the virtual address to a physical address. The memory is segmented into four regions by its access mode and caching capability as shown in the following table.

Table 14. Address Mapping

Segment	Size	Caching	Virtual Address Range	Physical Address Range	Mode
KUSEG	2048M	cacheable	0x0000_0000-0x7fff_ffff	Set in TLB	user/kernel
KSEG0	512M	cacheable	0x8000_0000-0x9fff_ffff	0x0000_0000-0x1fff_ffff	kernel
KSEG1	512M	uncachable	0xa000_0000-0xbfff_ffff	0x0000_0000-0x1fff_ffff	kernel
KSEG2	512M	cacheable	0xc000_0000-0xfeff_ffff	Set in TLB	kernel
KSEG2	512M	cacheable	0xff00_0000-0xffff_ffff	0xff00_0000-0xffff_ffff	kernel

The RTL8181 & RTL8181P have two memory mapping modes: direct memory mapping and TLB (Translation Look-aside Buffer) address mapping. When a virtual address is located in the regions KSEG0, KSEG1, or the higher half of the KSEG2 segment, its physical address is mapped directly from the virtual address with an offset. If a virtual address is used in the region of KUSEG or the lower half of the KSEG2 segment, its physical address will be referenced from a TLB entry. The RTL8181/RTL8181P contains 16 TLB entries, each of which maps to a page, with read/write access, cache-ability and process id.

SDRAM is mapped from physical address 0x0000_0000 to a maximum 0x01ff_ffff (32Mbytes). After reset, instructions are fetched from physical address 0x1fc0_0000, the starting address of flash memory. Flash memory is mapped from the physical address 0x1fc0_0000 to a maximum 0x1fff_ffff (4Mbytes).

6.1. Memory Map (Without TLB)

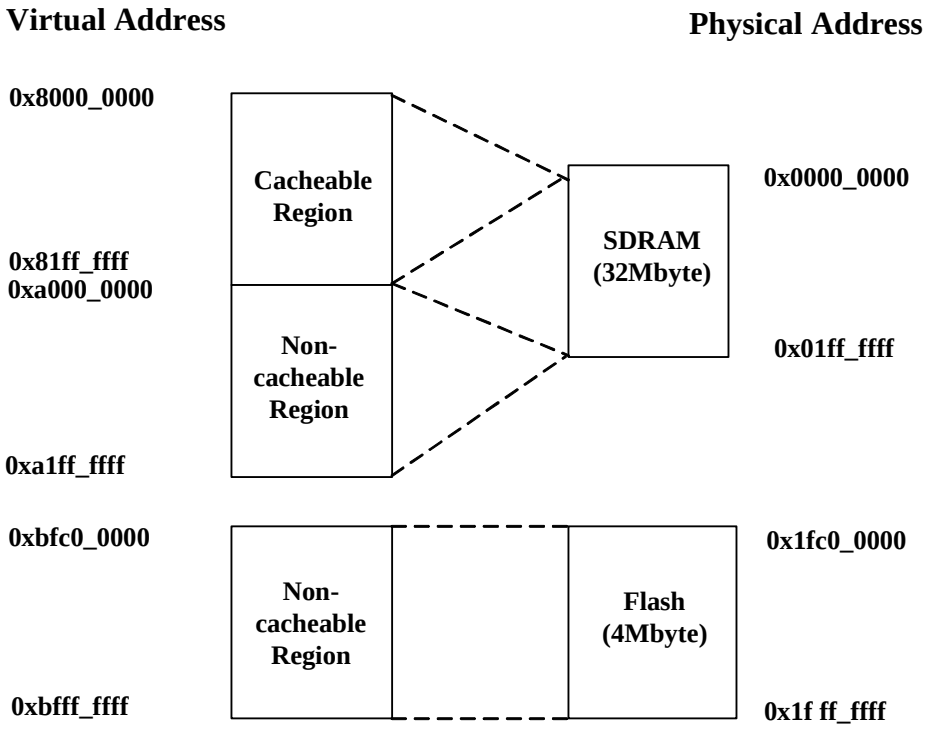


Figure 4. Memory Map (Without TLB)

The memory map of I/O devices and registers are located in the KSEG1 segment (non-cacheable region). Table 15 illustrates the address map.

Table 15. Memory Mapping

Virtual Address Range	Size (bytes)	Mapped Device
0xBD01_0000 – 0xBD01_0FFF	4K	Special function registers. Special functions include interrupt control, timer, watchdog, UART, and GPIO.
0xBD01_1000 – 0xBD01_1FFF	4K	Memory controller registers.
0xBD20_0000 – 0xBD2F_FFFF	1M	Ethernet0.
0xBD30_0000 – 0xBD3F_FFFF	1M	Ethernet1.
0xBD40_0000 – 0xBD4F_FFFF	1M	WLAN controller.
0xBD50_0000 – 0xBD5F_FFFF	1M	IO map address of PCI device.
0xBD60_0000 – 0xBD6F_FFFF	1M	Memory map address of PCI device.
0xBD70_0000 – 0xBD77_FFFF	512K	Configuration space of PCI device0.
0xBD78_0000 – 0xBD7F_FFFF	512K	Configuration space of PCI device1.

7. Register Mapping

Table 16 displays the address mapping of all registers.

Table 16. Register Mapping

Virtual Address	Register Symbol	Register Name
Interrupt Controller		
0xBD01_0000	GIMR	Global Interrupt Mask Register.
0xBD01_0004	GISR	Global Interrupt Status Register.
GPIO		
0xBD01_0040	PABDIR	Port A/B Direction Register.
0xBD01_0044	PABDATA	Port A/B Data Register.
0xBD01_0048	PBIMR	Port B Interrupt Mask Register.
0xBD01_004C	PBISR	Port B Interrupt Register.
Timer		
0xBD01_0050	TCCNT	Timer/Counter Control Register.
0xBD01_0054	TCIR	Timer/Counter Interrupt Register.
0xBD01_0058	CDBR	Clock Division Base Register.
0xBD01_005C	WDTCNR	Watchdog Timer Control Register.
0xBD01_0060	TC0DATA	Timer/Counter 0 Data register.
0xBD01_0064	TC1DATA	Timer/Counter 1 Data register.
0xBD01_0068	TC2DATA	Timer/Counter 2 Data register.
0xBD01_006C	TC3DATA	Timer/Counter 3 Data register.
0xBD01_0070	TC0CNT	Timer/Counter 0 Count register.
0xBD01_0074	TC1CNT	Timer/Counter 1 Count register.
0xBD01_0078	TC2CNT	Timer/Counter 2 Count register.
0xBD01_007C	TC3CNT	Timer/Counter 3 Count register.
UART		
0xBD01_00C3	UART_RBR	UART Receiver Buffer Register.
0xBD01_00C3	UART_THR	UART Transmitter Holding Register.
0xBD01_00C3	UART_DLL	UART Divisor Latch LSB.
0xBD01_00C7	UART_DLM	UART Divisor Latch MSB.
0xBD01_00C7	UART_IER	UART Interrupt Enable Register.
0xBD01_00CB	UART_IIR	UART Interrupt Identification Register.
0xBD01_00CB	UART_FCR	UART FIFO Control Register.
0xBD01_00CF	UART_LCR	UART Line Control Register.
0xBD01_00D3	UART_MCR	UART Modem Control Register.
0xBD01_00D7	UART_LSR	UART Line Status Register.
0xBD01_00DB	UART_MSR	UART Modem Status Register.
0xBD01_00DF	UART_SCR	UART Scratch Register.
System Config Register		
0xBD01_0100	BRIDGE_REG	WLAN, Ethernet0, Ethernet1 and PCI bridge configuration register.
0xBD01_0104	PLLMN_REG	DLL M ,N parameter.
0xBD01_0108	MEM_REG	Memory clock setting.
0xBD01_0109	CPU_REG	CPU clock setting.
Memory Controller		
0xBD01_1000	MCR	Memory Configuration Register.
0xBD01_1004	MTCR0	Memory Timing Configuration Register 0.
0xBD01_1008	MTCR1	Memory Timing Configuration Register 1.

Virtual Address	Register Symbol	Register Name
Ethernet0		
0xBD20_0000	ETH0_CNR1	Ethernet0 Control Register 0.
0xBD20_0004	ETH0_ID	Ethernet0 ID.
0xBD20_000C	ETH0_MAR	Ethernet0 Multicast Register.
0xBD20_0014	ETH0_TSAD	Ethernet0 Transmit Starting Address Descriptor.
0xBD20_0018	ETH0_RSAD	Ethernet0 Receive Starting Address Descriptor.
0xBD20_0020	ETH0_IMR	Ethernet0 Interrupt Mask Register.
0xBD20_0024	ETH0_ISR	Ethernet0 Interrupt Status Register.
0xBD20_0028	ETH0_TMF0	Ethernet0 Type Filter 0 register.
0xBD20_002C	ETH0_TMF1	Ethernet0 Type Filter 1 register.
0xBD20_0030	ETH0_TMF2	Ethernet0 Type Filter 2 register.
0xBD20_0034	ETH0_TMF3	Ethernet0 Type Filter 3 register.
0xBD20_0038	ETH0_MII	Ethernet0 MII access register.
0xBD20_003C	ETH0_CNR2	Ethernet0 Control Register 2.
0xBD20_0040	ETH0_UAR	Ethernet0 Unicast Address Register.
0xBD20_0080	ETH0_MPC	Ethernet0 Mismatch Packet Counter.
0xBD20_0083	ETH0_TXCOL	Ethernet0 Transmit Collision Counter.
0xBD20_0085	ETH0_RXER	Ethernet0 Receive Error count.
Ethernet1		
0xBD30_0000	ETH1_CNR1	Ethernet1 Control Register 0.
0xBD30_0004	ETH1_ID	Ethernet1 ID.
0xBD30_000C	ETH1_MAR	Ethernet1 Multicast Register.
0xBD30_0014	ETH1_TSAD	Ethernet1 Transmit Starting Address Descriptor.
0xBD30_0018	ETH1_RSAD	Ethernet1 Receive Starting Address Descriptor.
0xBD30_0020	ETH1_IMR	Ethernet1 Interrupt Mask Register.
0xBD30_0024	ETH1_ISR	Ethernet1 Interrupt Status Register.
0xBD30_0028	ETH1_TMF0	Ethernet1 Type Match Filter 0.
0xBD30_002C	ETH1_TMF1	Ethernet1 Type Match Filter 1.
0xBD30_0030	ETH1_TMF2	Ethernet1 Type Match Filter 2.
0xBD30_0034	ETH1_TMF3	Ethernet1 Type Match Filter 3.
0xBD30_0038	ETH1_MII	Ethernet1 MII access register.
0xBD30_003C	ETH1_CNR2	Ethernet1 Control Register 2.
0xBD30_0080	ETH1_MPC	Ethernet1 Mismatch Packet Counter.
0xBD30_0083	ETH1_TXCOL	Ethernet1 Transmit Collision counter.
0xBD30_0085	ETH1_RXER	Ethernet1 Receive Error count.
WLAN Controller		
0xBD40_0000	WLAN_ID	WLAN ID.
0xBD40_0008	WLAN_MAR	WLAN Multicast Register.
0xBD40_0018	WLAN_TSFTR	WLAN Timing Synchronization Function Timer Register.
0xBD40_0020	WLAN_TLPDA	WLAN Transmit Low Priority Descriptors start Address.
0xBD40_0024	WLAN_TNPDA	WLAN Transmit Normal Priority Descriptors start Address.
0xBD40_0028	WLAN_THPDA	WLAN Transmit High Priority Descriptors start Address.
0xBD40_002C	WLAN_BRSR	WLAN Basic Rate Set Register.
0xBD40_002E	WLAN_BSSID	WLAN Basic Service Set ID.
0xBD40_0037	WLAN_CR	WLAN Command Register.
0xBD40_003C	WLAN_IMR	WLAN Interrupt Mask Register.
0xBD40_003E	WLAN_ISR	WLAN Interrupt Status Register.
0xBD40_0040	WLAN_TCR	WLAN Transmit Configuration Register.
0xBD40_0044	WLAN_RCR	WLAN Receive Configuration Register.
0xBD40_0048	WLAN_TINT	WLAN Timer Interrupt register.

Virtual Address	Register Symbol	Register Name
0xBD40_004C	WLAN_TBDA	WLAN Transmit Beacon Descriptor start Address.
0xBD40_0050	WLAN_CR	WLAN Command Register.
0xBD40_0051	WLAN_CONFIG0	WLAN Configuration register 0.
0xBD40_0053	WLAN_CONFIG2	WLAN Configuration register 2.
0xBD40_0054	WLAN_ANAPARM	WLAN Analog parameter.
0xBD40_0058	WLAN_MSR	WLAN Media Status Register.
0xBD40_0059	WLAN_CONFIG3	WLAN Configuration register 3.
0xBD40_005A	WLAN_CONFIG4	WLAN Configuration register 4.
0xBD40_005B	WLAN_TESTR	WLAN Test mode Register.
0xBD40_005F	WLAN_SCR	WLAN Security Configuration Register.
0xBD40_0070	WLAN_BCNITV	WLAN Beacon Interval register.
0xBD40_0072	WLAN_ATIMWND	WLAN ATIM Window register.
0xBD40_0074	WLAN_BINTRITV	WLAN Beacon Interrupt Interval register.
0xBD40_0076	WLAN_ATIMTRITV	WLAN ATIM Interrupt Interval register.
0xBD40_0078	WLAN_PHYDELAY	WLAN PHY Delay register.
0xBD40_007A	WLAN_CRC16ERR	WLAN CRC16 Error count.
0xBD40_007C	WLAN_PHYADDR	WLAN PHY Address Register.
0xBD40_007D	WLAN_PHYDATAW	WLAN PHY Data Write.
0xBD40_007E	WLAN_PHYDATAR	WLAN PHY Data Read.
0xBD40_0080	WLAN_PHYCFG	WLAN PHY Configuration register.
0xBD40_0090	WLAN_DK0	WLAN Default Key 0 register.
0xBD40_00A0	WLAN_DK1	WLAN Default Key 1 register.
0xBD40_00B0	WLAN_DK2	WLAN Default Key 2 register.
0xBD40_00C0	WLAN_DK3	WLAN Default Key 3 register.
0xBD40_00D8	WLAN_CONFIG5	WLAN Configuration register 5.
0xBD40_00D9	WLAN_TPPOLL	WLAN Transmit Priority Polling register.
0xBD40_00DC	WLAN_CWR	WLAN Contention Window Register.
0xBD40_00DE	WLAN_RETRYCTR	WLAN Retry Count Register.
0xBD40_00E4	WLAN_RDSAR	WLAN Receive Descriptor Start Address Register.
0xBD40_0100	WLAN_KMAR	WLAN Key Map Address Register.
0xBD40_0106	WLAN_KMKEY	WLAN Key Map Key Value.
0xBD40_0116	WLAN_KMC	WLAN Key Map Configuration.

8. System Configuration

8.1. GPIO Pin for System Configuration

Table 17. GPIO Pin for System Configuration

GPIOB Pin	Power on Latch Value	Operating Setting	Power on Default
9-6	1111 Other values are reserved	CPU=200, MEM=100 if Memory uses asynchronous mode.	1111
11, 10	01 11 Other values are reserved	JTAG mode. Normal mode (WLAN LED).	11
13	1 0	Memory clock use asynchronous mode. Synchronous mode. The MEM clock is the same as the CPU clock.	1
15-14	Reserved	Reserved.	
1, 0	1, 1. Other values are reserved	Must be 1, 1 at power on state	1, 1

8.2. System Control Register Set

Table 18. System Control Register Set

Virtual Address	Size (byte)	Name	Description
0xBD01_0100	4	BRIDGE_REG	WLAN, Ethernet0, Ethernet1, and PCI bridge configuration Register.
0xBD01_0104	4	PLLMN_REG	DPLL parameter.
0xBD01_0108	1	MEM_REG	Memory clock rate.
0xBD01_0109	1	CPU_REG	CPU clock rate.

8.3. Bridge Control Register (BRIDGE_REG)

Since the Lexra bus clock rate is faster than the network device, it needs a bus bridge between the CPU and device (i.e., Ethernet and Wireless LAN controller). This bridge also exists between the CPU and PCI bridge.

Table 19. Bridge Control Register (BRIDGE_REG)

Bit	Bit Name	Description	RW	InitVal
2-0	NIC0CKR	Bus clock to NIC0 clock ratio. 001= 1:2, 011=1:4, 101=1:6, 111=1:8 Other values are reserved. NIC0 and NIC1 maximum clock is 50MHz.	RW	011
3	NIC0CKREN	NIC0CKR write enable.	RW	0
6-4		Reserved.		
7	DISNIC0B	Disable NIC0. 0: Enable NIC0 1: Disable NIC0	RW	0
10-8	NIC1CKR	Bus clock to NIC1 clock ratio. 001= 1:2, 011=1:4, 101=1:6, 111=1:8 Other values are reserved. NIC1 maximum clock is 50MHz.	RW	011
11	NIC1CKREN	NIC0CKR write enable	RW	0
14-12		Reserved.		

Bit	Bit Name	Description	RW	InitVal
15	DISNIC1B	Disable NIC1. 0: Enable NIC1 1: Disable NIC1	RW	0
18-16	PCICLKR	Bus clock to PCI clock ratio. 000=1:1, 001= 1:2, 010=1:3, 011=1:4, 100=1:5, 101=1:6, 110=1:7, 111=1:8. The PCI maximum clock is 50MHz.	RW	101
19	PCICKREN	PCICLKR write enable.	RW	0
20	LXPCI	External Bus is PCI or Lexra (debug mode). 0: Lexra 1: PCI	RW	1
21	PCI2ENB	Second PCI bus enable. 0: Enable second PCI device 1: Disable second PCI device	RW	1
22	Reserved			
23	DISPCIB	Disable PCI bridge. 0: Enable PCI bridge 1: Disable PCI bridge	RW	0
26-24	WLANCKR	Bus clock to WLAN clock ratio. 000=1:1, 001= 1:2, 010=1:3, 011=1:4, 100=1:5, 101=1:6, 110=1:7, 111=1:8. WLAN maximum clock is 40MHz.	RW	101
27	WLANCKREN	WLANCKR write enable.	RW	0
30-28	Reserved			
31	DISWLANB	Disable WLAN. 0: Enable WLAN 1: Disable WLAN	RW	0

8.4. DPLL M, N Parameter Register (PLLMN_REG)

The DPLL clock rate is set using this equation: 44MHz*(M+1)/(N+1).

Table 20. DPLL M, N Parameter Register (PLLMN_REG)

Bit	Bit Name	Description	RW	InitVal
4-0	NDIV	DPLL N parameter.	RW	00011
7-5	Reserved			
13-8	MDIV	DPLL M parameter.	RW	10011
14	MNEN	MDIV and NDIV write enable. 0: Disable 1: Enable	RW	0
31-15	Reserved			0

8.5. Memory Parameter Register (MEM_REG)

Table 21. Memory Parameter Register (MEM_REG)

Bit	Bit Name	Description	RW	InitVal
2-0	MEMDIV	MEM clock. 000:DPLL/1, 001:DPLL/1.5, 010:DPLL/2, 011:DPLL/2.5, 100:DPLL/3, 101:DPLL/4, 110:DPLL/6, 111:DPLL/8	RW	000
3	MEMDIVEN	Enable MEMDIV write. 0: Disable 1: Enable	RW	0
7-4	Reserved			

8.6. CPU Parameter Register (CPU_REG)

Table 22. CPU parameter Register (CPU_REG)

Bit	Bit Name	Description	RW	InitVal
2-0	CPUDIV	CPU clock. 000:DPLL/1, 001:DPLL/1.5, 010:DPLL/2, 011:DPLL/2.5, 100:DPLL/3, 101:DPLL/4, 110:DPLL/6, 111:DPLL/8	RW	000
3	CPUDIVEN	Enable CPUDIV write. 0: Disable 1: Enable	RW	0
7-4	Reserved			

9. Interrupt Controller

The RTL8181/RTL8181P provides six internal hardware-interrupt inputs (IRQ0-IRQ5). Some devices share the same IRQ signal. Table 23 displays the IRQ map used by devices.

Table 23. Interrupt Controller

IRQ Number	Interrupt Source
0	Timer/Counter interrupt.
1	GPIO/LBC interrupt.
2	WLAN interrupt.
3	UART/PCI interrupt.
4	Ethernet0 interrupt.
5	Ethernet1 interrupt.

There are two registers for interrupt control. The Global Interrupt Mask Register (Table 25) enables/disables the interrupt source. The Global Interrupt Status Register, Table 26, page 25 shows the pending interrupt status.

9.1. Interrupt Control Register Set

Table 24. Interrupt Control Register Set

Virtual address	Size (byte)	Name	Description
0xBD01_0000	2	GIMR	Global Interrupt Mask Register.
0xBD01_0004	2	GISR	Global Interrupt Status Register.

9.2. Global Interrupt Mask Register (GIMR)

Table 25. Global Interrupt Mask Register (GIMR)

Bit	Bit Name	Description	RW	InitVal
0	TCIE	Timers/Counters Interrupt Enable. 0: Disable 1: Enable	RW	0
1	GPIOIE	GPIO Interrupt Enable. 0: Disable 1: Enable	RW	0
2	WLAIE	WLAN controller Interrupt Enable. 0: Disable 1: Enable	RW	0
3	UARTIE	UART Interrupt Enable. 0: Disable 1: Enable	RW	0
4	ETH0IE	Ethernet0 Interrupt Enable. 0: Disable 1: Enable	RW	0
5	ETH1IE	Ethernet1 Interrupt Enable. 0: Disable 1: Enable	RW	0
6	PCIIE	PCI Interrupt Enable. 0: Disable 1: Enable	RW	0
7	Reserved			
8	LBCIE	LBC time-out Interrupt Enable. 0: Disable 1: Enable	RW	0

9.3. Global Interrupt Status Register (GISR)

Table 26. Global Interrupt Status Register (GISR)

Bit	Bit Name	Description	RW	InitVal
0	TCIP	Timers/Counters Interrupt Pending flag. 0: None Pending 1: Pending	R	0
1	GPIOIP	GPIO Interrupt Pending flag. 0: None Pending 1: Pending	R	0
2	WLAIP	WLAN controller Interrupt Pending flag. 0: None Pending 1: Pending	R	0
3	UARTIP	UARTI Interrupt Pending flag. 0: None Pending 1: Pending	R	0
4	ETH0IP	Ethernet0 Interrupt Pending flag. 0: None Pending 1: Pending	R	0
5	ETH1IP	Ethernet1 Interrupt Pending flag. 0: None Pending 1: Pending	R	0
6	PCIIP	PCI Interrupt Pending flag. 0: None Pending 1: Pending	R	0
7	Reserved			
8	LBCIP	LBC time-out Interrupt Pending flag. 0: None Pending 1: Pending	R	0

10. Memory Controller

A memory control module provides access to external asynchronous SDRAM and flash memory.

The RTL8181/RTL8181P interfaces with PC100 or PC133-compliant SDRAM, and supports auto-refresh mode, which requires a 4096-cycle refresh in 64 ms. The SDRAM can be accessed in two banks (CS0# and CS1#), and its size and timing are configurable via the registers. The data width of SDRAM may be set to either 16-bit or 32-bit. If configured as 32-bit, either one bank of 32-bit SDRAM, or two banks of 16-bit SDRAM may be used to expand the data width to 32 bits.

The RTL8181/RTL8181P also supports two-bank access for flash memory (F_CS0# and F_CS1#). The system will always boot from bank 0. The boot bank is mapped to KSEG1 and its beginning virtual address is 0xBFC0_0000 (physical address: 0x1FC0_0000). Bank 1 flash memory will be mapped to the address '0x1FC0_000 + flash size'. The flash size is configurable from 1M to 8Mbytes for each bank. If the flash size is greater than 4M, the first 4M will be still mapped to address 0xBFC0_000 to 0xBFCF_FFFF, and the others will be mapped from the virtual address 0xBE00_0000.

10.1. Memory Configuration Register Set

Table 27. Memory Configuration Register Set

Virtual Address	Size (byte)	Name	Description
0xBD01_1000	4	MCR	Memory Configuration Register
0xBD01_1004	4	MTCR0	Memory Timing Configuration Register 0
0xBD01_1008	4	MTCR1	Memory Timing Configuration Register 1

Note: These three registers should be accessed in double word.

10.2. Memory Configuration Register (MCR)

Table 28. Memory Configuration Register (MCR)

Bit	Bit Name	Description	RW	InitVal
31-30	FLSIZE	Flash Size respective to one bank (byte). 00: 1M, 01: 2M, 10: 4M, 11: 8M	RW	11
29-28	SDRSIZE	SDRAM Size respective to one bank (bit). 00: 512Kx16x2, 01: 1Mx16x4, 10: 2Mx16x4, 11:Reserved	RW	01
27	CAS	CAS latency. 0: Latency=2 1: Latency=3	RW	0
26-25	FLBK0BW	Flash Bank 0 Bus Width. 01: 16 bit	R	
24-23	FLBK1BW	Flash Bank 1 Bus Width. 00 11 10: reserved, 01: 16 bit	RW	01
22-21		Reserved.		
20	SDBUSWID	SDRAM Bus Width. 0: 16 bit 1: 32 bit	RW	0
19	MCK2LCK	Memory Clock mode. Power on latch from GPIOB[13]. 1: Memory clock is the same as CPU clock. 0: Memory clock follows the power on latch from SYSCFG[3-0].	R	

Bit	Bit Name	Description	RW	InitVal
18-16	BUSCLK	Bus Clock to control auto-refresh timing. 000:200, 001:100, 010:50, 011:25, 100:12.5, 101:6.25 110:3.125, 111:1.5625 MHz	RW	000
15-0	Reserved	Must be set to bit value 00.	RW	00

10.3. Memory Timing Configuration Register 0 (MTCR0)

Table 29. Memory Timing Configuration Register 0 (MTCR0)

Bit	Bit Name	Description	RW	InitVal
31-28	CE0T_CS	The timing interval between F_CE0# and WR#. Basic unit = 2*clock cycle. '0000' means 1 unit (2 clock cycles).	RW	1111
27-24	CE0T_WP	The timing interval for WR# to be pulled-low. Basic unit = 2*clock cycle '0000' means 1 unit (2 clock cycles).	RW	1111
23-20	CE1T_CS	The timing interval between F_CE1# and WR#. Basic unit = 2*clock cycle '0000' means 1 unit (2 clock cycles).	RW	1111
19-16	CE1T_WP	The timing interval for WR# to be pulled-low. Basic unit = 2*clock cycle '0000' means 1 unit (2 clock cycles).	RW	1111
15-0		Reserved.		

Note: The clock cycle is memory clock based.

10.4. Memory Timing Configuration Register 1 (MTCR1)

Table 30. Memory Timing Configuration Register 1 (MTCR1)

Bit	Bit Name	Description	RW	InitVal
12-10	CE23T_RP=T_RCD	T_RP and T_RCD timing parameter. Basic unit = 1*clock cycle '0000' means 1 unit (1 clock cycle).	RW	111
9-5	CE23T_RAS	T_RAS timing parameter. Basic unit = 1*clock cycle '0000' means 1 unit (1 clock cycle).	RW	11111
4-0	CE23T_RFC	T_RFC timing parameter for refresh interval. Basic unit = 1*clock cycle '0000' means 1 unit (1 clock cycle).	RW	11111

Note: The clock cycle is memory clock based.

10.5. SDRAM Timing

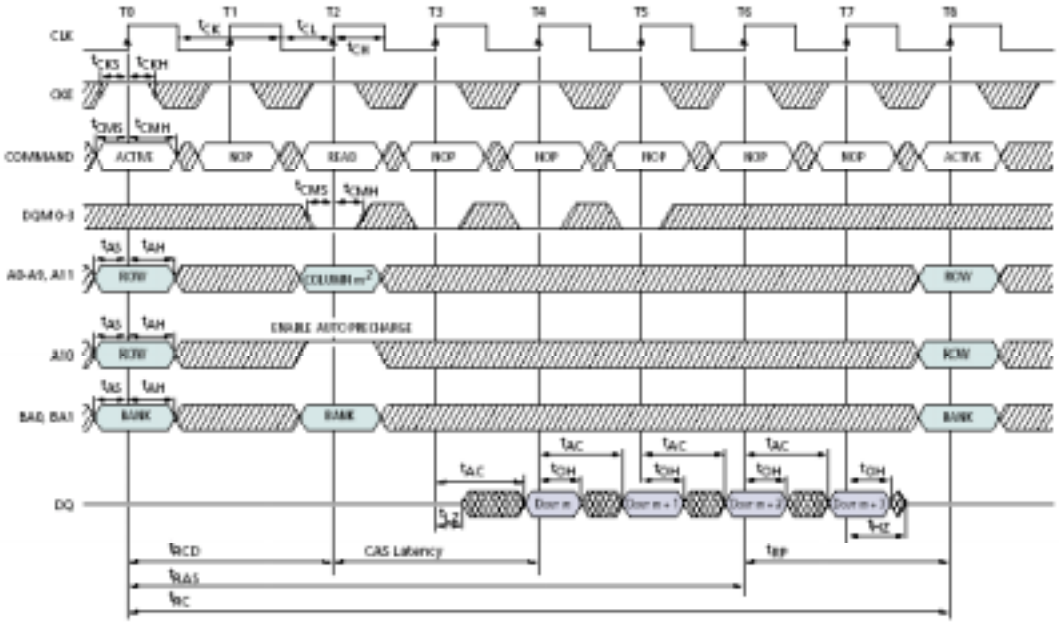


Figure 5. SDRAM Timing

10.6. Flash Memory Write Access Timing

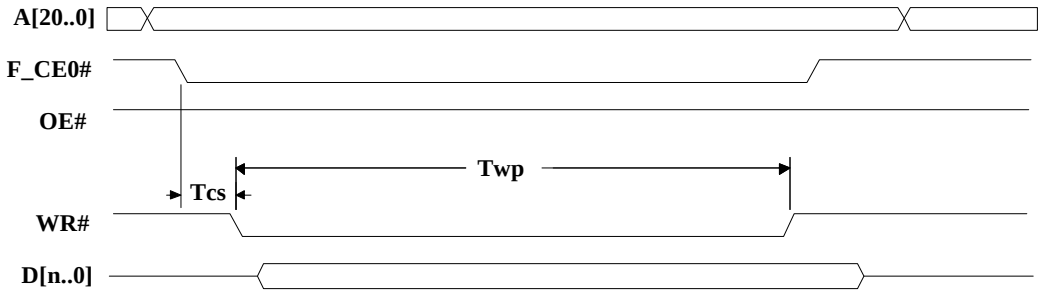


Figure 6. Flash Memory Write Access Timing

10.7. Flash Memory Read Access Timing

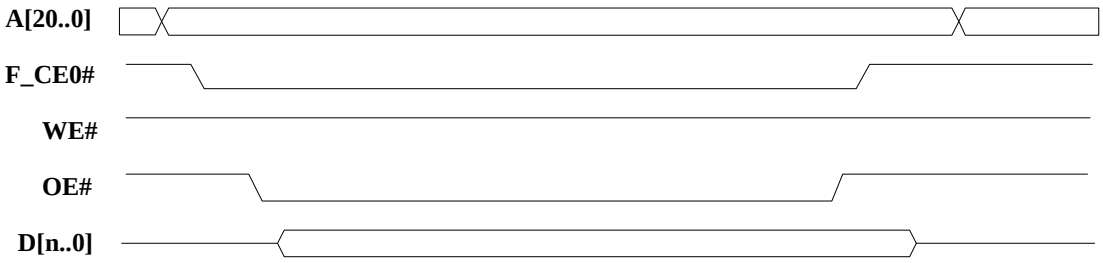


Figure 7. Flash Memory Read Access Timing

11. Ethernet Controller

There are two 10/100M Ethernet MACs embedded in the RTL8181/RTL8181P. The Ethernet device has bus master capability and moves packets between SDRAM and the Ethernet controller through a DMA mechanism, lessening the CPU loading and giving better performance. It also supports full-duplex operation, making 200Mbps bandwidth possible for no additional cost.

11.1. Ethernet 0 Register Set

Table 31. Ethernet 0 Register Set

Virtual Address	Size (byte)	Name	Description	Access
0xBD20_0000	4	ETH0_CNR1	Control Register 1.	RW
0xBD20_0004	6	ETH0_ID	NIC ID.	RW
0xBD20_000C	8	ETH0_MAR	Multicast Register.	RW
0xBD20_0014	4	ETH0_TSAD	Transmit Starting Logic Address of Descriptor.	RW
0xBD20_0018	4	ETH0_RSAD	Receive Starting Logic Address of Descriptor.	RW
0xBD20_0020	2	ETH0_IMR	Ethernet0 Interrupt Mask Register.	RW
0xBD20_0024	2	ETH0_ISR	Ethernet0 Interrupt Status Register.	RW
0xBD20_0028	4	ETH0_TMF0	Type Match Filter 0 register.	RW
0xBD20_002C	4	ETH0_TMF1	Type Match Filter 1 register.	RW
0xBD20_0030	4	ETH0_TMF2	Type Match Filter 2 register.	RW
0xBD20_0034	4	ETH0_TMF3	Type Match Filter 3 register.	RW
0xBD20_0038	4	ETH0_MII	MII access register.	RW
0xBD20_003C	4	ETH0_CNR2	NIC control Register 2.	RW
0xBD20_0040	16	ETH0_UAR	Unicast Address filter Register.	RW
0xBD20_0080	3	ETH0_MPC	Indicates the number of packets discarded due to Rx FIFO overflow. This is a 24-bit counter and is cleared to zero by the read command.	R
0xBD20_0084	2	ETH0_TXCOL	Transmit Collision counter. This 16-bit counter increments by 1 for every collision event. It rolls over when becomes full. It is cleared to zero by the read command.	R
0xBD20_0088	2	ETH0_RXER	Receive error count. This 16-bit counter increments by 1 for each valid packet received. It is cleared to zero by the read command.	R

11.2. Ethernet 1 Register Set

Table 32. Ethernet 1 Register Set

Virtual Address	Size (byte)	Name	Description	Access
0xBD30_0000	4	ETH1_CNR1	Control Register 1.	RW
0xBD30_0004	6	ETH1_ID	NIC ID.	RW
0xBD30_000C	8	ETH1_MAR	Multicast Register.	RW
0xBD30_0014	4	ETH1_TSAD	Transmit Starting Logic Address of Descriptor.	RW
0xBD30_0018	4	ETH1_RSAD	Receive Starting Logic Address of Descriptor.	RW
0xBD30_0020	2	ETH1_IMR	Ethernet0 Interrupt Mask Register.	RW
0xBD30_0024	2	ETH1_ISR	Ethernet0 Interrupt Status Register.	RW
0xBD30_0028	4	ETH1_TMF0	Type Match Filter 0 register.	RW
0xBD30_002C	4	ETH1_TMF1	Type Match Filter 1 register.	RW

Virtual Address	Size (byte)	Name	Description	Access
0xBD30_0030	4	ETH1_TMF2	Type Match Filter 2 register.	RW
0xBD30_0034	4	ETH1_TMF3	Type Match Filter 3 register.	RW
0xBD30_0038	4	ETH1_MII	MII access register.	RW
0xBD30_003C	4	ETH1_CNR2	NIC Control Register 2.	RW
0xBD30_0080	3	ETH1_MPC	Indicates the number of packets discarded due to Rx FIFO overflow. It is a 24-bit counter. It is cleared to zero by the read command.	R
0xBD30_0084	2	ETH1_TXCOL	Transmit Collision counter. This 16-bit counter increments by 1 for every collision event. It rolls over when it becomes full. It is cleared to zero by the read command.	R
0xBD30_008C	2	ETH1_RXER	Receive Error count. This 16-bit counter increments by 1 for each valid packet received. It is cleared to zero by the read command.	R

11.3. Ethernet Control Register 1 (ETH0_CNR1, ETH1_CNR1)

Table 33. Ethernet Control Register 1 (ETH0_CNR1, ETH1_CNR1)

Bit	Bit Name	Description	RW	InitVal
31-29	RXBLEN	Rx Burst Length on Lexra bus. 000 - 010 = 64 bytes	RW	000
28-26	TXBLEN	Tx Burst Length on Lexra bus. 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes	RW	000
25	Reserved			
24	TDFN	Tx Descriptor Fetch Notify. Set this bit to notify the NIC to fetch the Tx descriptors. The NIC will clear this bit automatically after all packets have been transmitted. Writing 0 to this bit has no effect.	W	0
20	RST	Reset. A soft reset that disables the transmitter and receiver, and re-initializes the FIFOs and buffer pointer to the initial values.	W	0
19	RE	Receiver Enable.	RW	0
18	TE	Transmitter Enable.	RW	0
17	TxFCE	Transmit Flow Control Enable.	RW	0
16	RxFCE	Receive Flow Control Enable.	RW	0
15	Reserved			0
14	RxVLAN	Receive VLAN un-tagged enable.	RW	0
13	RxChkSum	Receive Checksum offload enable.	RW	0
12	FSWInt	Forced Software Interrupt. Writing 1 to this bit will trigger an interrupt and the SWIP bit will be set. The NIC will clear this bit automatically after the SWIP bit is cleared. Writing 0 to this bit has no effect.	W	
11-10	LBK[1:0]	Loopback test. Setting both bits will route all transmit traffic from Tx FIFO to Rx FIFO. 00: Normal operation 01, 10: Reserved 11: Loopback mode	RW	00

Bit	Bit Name	Description	RW	InitVal
9	NoCRC	No CRC. 0: CRC appended 1: No CRC appended	RW	0
8	AER	Accept Error packets.	RW	0
7	AB	Accept Broadcast packets.	RW	0
6	AM	Accept Multicast packets.	RW	0
5	APM	Accept Physical address Matched packets.	RW	0
4	AAP	Accept All Physical packets.	RW	0
3	ATM	Accept Type Match packets. This bit enables the qualification of types of received packets.	RW	0
2	AR	Accept Runt packets.	RW	0
1	ALEN	Accept Length specific packets. This bit is effective when the ATM bit is set. 0: Filter length specific packets. 1: Accept length specific packets.	RW	0

11.4. Ethernet Control Register 2 (ETH0_CNR2, ETH1_CNR2)

Table 34. Ethernet Control Register 2 (ETH0_CNR2, ETH1_CNR2)

Bit	Bit Name	Description	RW	InitVal
16	UAEN	Unicast Address filter Enable. 0: Disabled. 1: Enabled. *Note: Bit UAEN only exists in the ETH0_CNR2 register.*	RW	0
15	TXPON	Transmit Pause On packet. Write '1' to send Pause On packet.	W	0
14	TXPOFF	Transmit Pause Off packet. Write '1' to send Pause Off packet.	W	0
13	TXPF	Transmit Pause Flag. Set when NIC sends Pause-On packet. Reset when NIC sends Pause-Off packet.	R	0
12	RXPF	Receive Pause Flag. Set when the NIC is in backoff state because a pause packet was received. Reset when the pause state is clear.	R	0
11-8	PTMASK[3:0]	Pause Time Mask. These bits mask the most significant four bits of pause time 0xFFFF used for a PAUSE packet. For example, if PTMASK[3:0] is set to 0x01, a PAUSE packet with pause time 0x1FFF will be sent when a descriptor unavailable condition occurs.	RW	1111

Bit	Bit Name	Description	RW	InitVal
6-4	IFG[2:0]	InterFrame Gap time. This field allows the user to adjust the InterFrame Gap time to longer than the standard: 9.6 us for 10Mbps, 960 ns for 100Mbps. The time can be programmed from 9.6 us to 14.4 us (10Mbps) and 960ns to 1440ns (100Mbps). The settings for the InterFrame Gap are: 011: 9.6us/960ns 100: 9.6+4*0.1us/960+4*10ns 101: 9.6+8*0.1us/960+8*10ns 110: 9.6+12*0.1us/960+12*10ns 111: 9.6+16*0.1us/960+16*10ns 000: 9.6+20*0.1us/960+20*10ns 001: 9.6+24*0.1us/960+24*10ns 010: 9.6+48*0.1us/960+48*10ns	RW	011
3-0	TXRR[3:0]	Tx Retry count. These are used to specify additional transmission retries in multiples of 16 (IEEE 802.3 CSMA/CD retry count). If the TXRR is set to 0, the transmitter will re-transmit 16 times before aborting due to excessive collisions. If the TXRR is set to a value greater than 0, the transmitter will re-transmit a number of times equal to the following formula before aborting: Total retries = 16 + (TXRR * 16) The TER bit in the ISR register or transmit descriptor will be set when the transmission fails and reaches this specified retry count.	RW	0

11.5. Unicast Address Filter Register (ETH0_UAR)

This register is used to filter unicast addresses of received packets. When this feature is enabled (ETH0_CNR2: UAEN is asserted), the RTL8181/RTL8181P will do a hash comparison of the DID (Destination ID) field of incoming unicast packets. It will take the seven Most Significant Bits (MSB) of MPDU-CRC32 as the hash index. If the bit value of ETH0_UAR is asserted, the incoming packet will be allowed; otherwise it will be discarded.

Table 35. Unicast Address Filter Register (ETH0_UAR)

Bit	Bit Name	Description	RW	InitVal
127-0	UARTBL	Unicast Address hash Table. If the ‘n’ bit value is set to ‘1’, received frames with a hash value of ‘n’ will be accepted.	RW	0

11.6. Interrupt Mask Register (ETH0_IMR, ETH1_IMR)

Table 36. Interrupt Mask Register (ETH0_IMR, ETH1_IMR)

Bit	Bit Name	Description	RW	InitVal
9	LINKCHGIE	Link status Change Interrupt Enable.	RW	0
8	RERIE	Rx Error Interrupt Enable.	RW	0
7	TERIE	Tx Error Interrupt Enable.	RW	0
6	ROKIE	ROK Interrupt Enable. Receive OK message (ROK). A descriptor reception has completed successfully.	RW	0
5	TOKIE	TOK Interrupt Enable. Transfer OK message (TOK). A descriptor transmission has completed successfully.	RW	0
4	RFOVWIE	Rx FIFO Overflow Interrupt Enable.	RW	0
3	RDUIE	Rx Descriptor Unavailable Interrupt Enable. Set when the Rx Descriptors have been exhausted.	RW	0
2	Reserved			
1	TDUIE	Tx Descriptor Unavailable Interrupt Enable.	RW	0
0	SWIE	Software Interrupt Enable.	RW	0

11.7. Interrupt Status Register (ETH0_ISR, ETH1_ISR)

Table 37. Interrupt Status Register (ETH0_ISR, ETH1_ISR)

Bit	Bit Name	Description	RW	InitVal
9	LINKCHGIP	Link status Change Interrupt Pending flag. Write ‘1’ to clear the interrupt.	RW	0
8	RERIP	Rx Error Interrupt Pending flag. Write ‘1’ to clear the interrupt.	RW	0
7	TERIP	Tx Error Interrupt Pending flag. Write ‘1’ to clear the interrupt.	RW	0
6	ROKIP	ROK Interrupt Pending. A descriptor reception has completed successfully. Write ‘1’ to clear the interrupt.	RW	0
5	TOKIP	TOK Interrupt Pending. A descriptor transmission has completed successfully. Write ‘1’ to clear the interrupt.	RW	0
4	RFOVWIP	Rx FIFO Overflow Interrupt Pending Write ‘1’ to clear the interrupt.	RW	0
3	RDUIP	Rx Descriptor Unavailable Interrupt Pending. Set when the Rx Descriptors have been exhausted. Write ‘1’ to clear the interrupt and trigger the NIC to send a PAUSE 0x0000 packet.	RW	0
2	Reserved			
1	TDUIP	Tx Descriptor Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	RW	0
0	SWIP	Software Interrupt Pending flag. Write ‘1’ to clear the interrupt.	RW	0

11.8. MII Access Register (ETH0_MII, ETH1_MII)

Table 38. MII Access Register (ETH0_MII, ETH1_MII)

Bit	Bit Name	Description	RW	InitVal
31-22		Reserved.		
21	MMIMODE	MII Management Interface Mode. 0: Auto mode. The NIC controls MDC and MDIO pins. Setting this bit will trigger an auto-negotiation if the DisNway bit is cleared. 1: Manual mode. The software controls MDC and MDIO pins.	RW	0
20-16	PHYAD[4:0]	PHY Address.	RW	0x01
15	LinkCtrl	Link Control. 0: Force link down 1: Force link up	RW	0
14	DplxCtrl	Duplex Control. 0: Force half-duplex mode 1: Force full-duplex mode	RW	1
13	SpdCtrl	Speed Control. 0: 10Mbps 1: 100Mbps	RW	1
12	FlCtrl	Flow Control. 0: Disable flow control 1: Enable flow control	RW	0
11	LinkSt	Link Status. This bit reflects the link status of its local PHY. 0: Link down 1: Link up	R	0
10	DuplexSt	Duplex Status. This bit reflects the duplex status of its local PHY. 0: Half duplex	R	0
9	SpeedSt	Speed Status. This bit reflects the link speed of its local PHY. 0: 10Mbps 1: 100Mbps	R	0
8	FlCtrlSt	Flow Control Status. 0: Flow control disabled 1: Flow control enabled	R	0
7-5		Reserved.		
4	DisNway	Disable NWay auto-negotiation. 0: Auto-negotiation mode. The local PHY will advertise its capability per the settings of DplxCtrl, SpdCtrl, and FlCtrl bits 1: Forced mode (disable NWay). The software may force MII operating mode by writing the corresponding value to the DplxCtrl, LinkCtrl, SpdCtrl, and FlCtrl bits	RW	0
3	MDM	Management Data Mode. 0: MDIO pin is input. The MDI bit reflects the state of the MDIO pin. The default value is ‘0’ 1: MDIO pin is output. The MDO bit reflects the state of the MDIO pin	RW	0
2	MDO	MII Management Data-OUT. Used by the NIC to write data to the MDIO pin.	RW	N/A
1	MDI	MII Management Data-IN. Used by the NIC to read data from the MDIO pin.	R	N/A
0	MDC	Management Data Clock. This bit reflects the state of the MDC pin.	RW	0

12. Transmission Descriptor

12.1. Tx Command Descriptor Format

Tx Descriptor Format (before transmitting, OWN=1, LGSEN=0, Tx command mode 1).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OWN=1	EOR	FS	LS	LGSEN=0	RESV	RESV	RESV	RESV	RESV	RESV	RESV	RESV	IPCS	UDPCS	TCPCS	Frame_Length																Offset 0
RESV														TAGC		VLAN_TAG																Offset 4
TX_BUFFER_ADDRESS																																Offset 8
Dummy																																Offset 12

Figure 8. Transmission Descriptor Format

Table 39. Transmission Descriptor

Byte Offset#	Bit#	Bit Name	Description
0	31	OWN	When set, indicates that the descriptor is owned by the NIC and the data relative to this descriptor is ready to be transmitted. When cleared, indicates that the descriptor is owned by the host system. The NIC clears this bit when the related buffer data is transmitted.
0	30	EOR	End Of descriptor Ring. When set, indicates that this is the last descriptor in the descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data related to this descriptor.
0	29	FS	First Segment descriptor. When set, indicates that this is the first descriptor of a Tx packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment descriptor. When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27	LGSEN	A command bit. TCP/IP-Large-Send operation enable. The driver sets this bit to enable the NIC to offload TCP/IP fragmentation operation to the CPU.
0	26-19		
0	18	IPCS	A command bit. IP Checksum offload. The driver sets this bit to ask the NIC to offload IP checksum operation.
0	17	UDPCS	A command bit. UDP Checksum offload. The driver sets this bit to ask the NIC to offload UDP checksum operation.

Byte Offset#	Bit#	Bit Name	Description
0	16	TCPCS	A command bit. TCP Checksum offload enable. The driver sets this bit to ask the NIC to offload TCP checksum operation.
0	15-0	Frame_Length	Transmit Frame Length. This field indicates the data length in the Tx buffer, in bytes, to be transmitted.
4	31-18	RSEV	Reserved.
4	17-16	TAGC	VLAN Tag Control bits. 00: Packet remains unchanged when transmitting 10: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is an IEEE 802.1Q VLAN packet) is inserted after the source address, and 2 bytes are inserted after the tag protocol ID in the VLAN_TAG field in the transmit descriptor.
4	15-0	VLAN_TAG	This 2-byte VLAN_TAG contains upper layer information; i.e., user priority, canonical format indicator, and VLAN ID. Refer to IEEE 802.1Q for detailed VLAN tag information.
8	31-0	TxBuff	Transmission Buffer logic address.

Note: After transmitting, the Tx descriptor becomes a Tx status descriptor.

12.2. Transmit Status Descriptor

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th></th></tr>
<tr><td>OWN=0</td><td>EOR</td><td>FS</td><td>LS</td><td>RESV</td><td>RESV</td><td>UNF</td><td>RESV</td><td>TES</td><td>OWC</td><td>LNKF</td><td>EXC</td><td colspan="4">CC3-0</td><td colspan="16">Frame_Length</td><td>Offset 0</td></tr>
<tr><td colspan="15">RESV</td><td>TAGC</td><td colspan="16">VLAN_TAG</td><td>Offset 4</td></tr>
<tr><td colspan="32">TX_BUFFER_ADDRESS</td><td>Offset 8</td></tr>
<tr><td colspan="32">Dummy</td><td>Offset 12</td></tr>
</table>

Figure 9. Transmit Status Descriptor Format

Table 40. Transmit Status Descriptor

Byte Offset#	Bit#	Bit Name	Description
0	31	OWN	When set, indicates that the descriptor is owned by the NIC. When clear indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data has been transmitted. In this case, OWN=0.
0	30	EOR	End Of descriptor Ring. When set, indicates that this is the last descriptor in the descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer returns to the first descriptor of the descriptor ring after transmitting the data related to this descriptor.
0	29	FS	First Segment descriptor. When set, indicates that this is the first descriptor of a Tx packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment descriptor. When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27-26		Reserved.
0	25	UNF	Under Run FIFO. A status bit. The NIC sets this bit to inform the driver that a FIFO under run occurred before this packet was transmitted.
0	24		Reserved.
0	23	TES	Transmit Error Summary. When set, indicates that at least one of the following errors occurred: OWC, EXC, LNKF. This bit is valid only when the LS (Last Segment) bit is set.
0	22	OWC	Out of Window Collision. A status bit. When set, it means an 'out-of-window' collision was encountered during packet transmission.
0	21	LNKF	Link Failure. A status bit. The NIC sets this bit to inform the driver of link failure.
0	20	EXC	Excessive Collisions. When set, indicates that the transmission was aborted owing to 16 consecutive collisions.
0	19-16	CC3-0	Collision Counter. When Own bit =0, this is a status field. A 4-bit collision counter that shows the number of collisions before the packet was finally transmitted.
0	23-16		Reserved.
0	15-0	Frame_ Length	Transmit Frame Length. This field indicates the length of data in the Tx buffer (in bytes) to be transmitted
4	31-18	RSEV	Reserved.
4	17-16	TAGC	VLAN Tag Control bits. 00: Packet remains unchanged when transmitting. 10: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is an IEEE 802.1Q VLAN packet) is inserted after the source address, and 2 bytes are inserted after the tag protocol ID in the VLAN_TAG field transmit descriptor.
4	15-0	VLAN_ TAG	The 2-byte VLAN_TAG contains upper layer information, i.e., user priority, canonical format indicator, and VLAN ID. Refer to IEEE 802 1Q for detailed VLAN tag information.
8	31-0	TxBuff	Transmission Buffer logic address.

13. Reception Descriptor

13.1. Rx Command Descriptor Format (OWN=1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OWN=1	EOR	RESV																	Buffer_Size													Offset 0
RESV															TAVA	VLAN_TAG																Offset 4
RX_BUFFER_ADDRESS																																Offset 8
Dummy																																Offset 12

Figure 10. Rx Command Descriptor Format (OWN=1)

Table 41. Rx Command Descriptor (OWN=1)

Bye Offset#	Bit#	Bit Name	Description
0	31	OWN	When set, indicates that the descriptor is owned by the NIC, and is ready to receive a packet. The OWN bit is set by the driver after pre-allocating buffers at initialization, or the host has released the buffer to the driver. In this case, OWN=1.
0	30	EOR	End Of Rx descriptor Ring. Set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used.
0	29-13		Reserved.
0	12-0	Buffer_Size	Buffer Size in bytes. Although the maximum buffer size is 8K bytes/buffer, the NIC purges all data after 4K bytes if the packet is larger than 4K-byte long.
4	31-17	RSEV	Reserved.
4	16	TAVA	Tag Available. When set, the received packet is an IEEE 802.1Q VLAN TAG (0x8100) available packet.
4	15-0	VLAN_TAG	If the packet's TAG is 0x8100, the NIC extracts four bytes from after the source ID, sets the TAVA bit to 1, and moves the TAG value to this field in the Rx descriptor.
8	31-0	RxBuff	Receive Buffer logic address.

13.2. Rx Status Descriptor (OWN=0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OWN=0	EOR	FS	LS	FAE	MAR	PAM	BAR	BOVF	FOVF	RWT	RES	RUNT	CRC	PID1	PID0	IPF	UDPF	TCPF	Frame_Length													Offset 0
RESV															TAVA	VLAN_TAG																Offset 4
RX_BUFFER_ADDRESS																																Offset 8
Dummy																																Offset 12

Figure 11. Rx Status Descriptor Format (OWN=0)

Table 42. Rx Status Descriptor (OWN=0)

Bye Offset#	Bit#	Bit Name	Description
0	31	OWN	When set, indicates that the descriptor is owned by the NIC. When cleared, indicates that the descriptor is owned by the host system. The NIC clears this bit when it has filled up this Rx buffer with a packet or part of a packet. In this case, OWN=0.
0	30	EOR	End of Rx descriptor Ring. Set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used for packet reception.
0	29	FS	First Segment descriptor. When set, indicates that this is the first descriptor of a received packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment descriptor. When set, indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet.
0	27	FAE	Frame Alignment Error. When set, indicates a frame alignment error has occurred on the received packet. An FAE packet can only be received when RCR_AER is set.
0	26	MAR	Multicast Address packet Received. When set, indicates that a multicast packet has been received.
0	25	PAM	Physical Address Matched. When set, indicates that the destination address of this Rx packet matches the value in the NIC's ID registers.
0	24	BAR	Broadcast Address Received. When set, indicates that a broadcast packet has been received. BAR and MAR cannot be set simultaneously.
0	23	BOVF	Buffer Overflow. When set, indicates that the receive buffer was exhausted before this packet was received.

Bye Offset#	Bit#	Bit Name	Description
0	22	FOVF	FIFO Overflow. When set, indicates that FIFO overflow occurred before this packet was received.
0	21	RWT	Receive Watchdog Timer expired. When set, indicates that the received packet length exceeded 1724 bytes, the receive watchdog timer expired and stopped the receive engine.
0	20	RES	Receive Error Summary. When set, indicates at least one of the following errors occurred: CRC, RUNT, RWT, FAE. This bit is valid only when the LS (Last Segment) bit is set.
0	19	RUNT	Runt packet. When set, indicates that the received packet length is smaller than 64 bytes. RUNT packets may only be received when RCR_AR is set.
0	18	CRC	CRC error. When set, indicates that a CRC error has occurred on the received packet. A CRC-error packet may only be received when RCR_AER is set.
0	17-16	PDI[1:0]	Protocol ID1, Protocol ID0 00: Non-IP 01: TCP/IP 10: UDP/IP 11: IP
0	15	IPF	When set, indicates IP checksum Failure.
0	14	UDPF	When set, indicates UDP checksum Failure.
0	13	TCPF	When set, indicates TCP checksum Failure.
0	12-0	Frame_ Length	When OWN=0 and LS =1, it shows the received packet length including CRC, in bytes.
4	31-17	RSEV	Reserved.
4	16	TAVA	Tag Available. When set, the received packet is an IEEE 802.1Q VLAN TAG (0x8100) available packet.
4	15-0	VLAN_ TAG	If the packet's TAG is 0x8100, the NIC extracts four bytes from after the source ID, sets the TAVA bit to 1, and moves the TAG value to this field in the Rx descriptor.
8	31-0	RxBuff	Receive Buffer logic address.

14. UART Controller

The RTL8181/RTL8181P features a 16C550 compatible UART containing a 16-byte FIFO buffer. In addition, auto flow control is provided, in which auto-CTS mode (CTS controls transmitter) and auto-RTS mode (Receiver FIFO contents and threshold control RTS) are both supported. The baud rate is programmable and allows division of any input reference clock by 1 to (2^16-1) and generates an internal 16x clock. The RTL8181/RTL8181P provides a fully programmable serial interface, which can be configured to support 7 or 8 bit characters, even, odd, or no parity generation and detection, and 1 or 2 stop bits generation. Fully prioritized interrupt control and loopback functionality for diagnostic purposes are also provided. The clock source is 22MHz.

14.1. UART Register Set

Table 43. UART Register Set

Virtual Address	Size (byte)	Name	Description	Access
0xBD01_00C3	1	UART_RBR	Receiver Buffer Register (DLAB=0).	R
0xBD01_00C3	1	UART_THR	Transmitter Holding Register (DLAB=0).	W
0xBD01_00C3	1	UART_DLL	Divisor Latch LSB (DLAB=1).	RW
0xBD01_00C7	1	UART_IER	Interrupt Enable Register (DLAB=0).	RW
0xBD01_00C7	1	UART_DLM	Divisor Latch MSB (DLAB=1).	RW
0xBD01_00CB	1	UART_IIR	Interrupt Identification Register.	R
0xBD01_00CB	1	UART_FCR	FIFO Control Register.	W
0xBD01_00CF	1	UART_LCR	Line Control Register.	RW
0xBD01_00D3	1	UART_MCR	Modem Control Register.	RW
0xBD01_00D7	1	UART_LSR	Line Status Register.	RW
0xBD01_00DB	1	UART_MSR	Modem Status Register.	RW
0xBD01_00DF	1	UART_SCR	Scratch Register.	RW

14.2. Interrupt Enable Register (UART_IER)

Table 44. Interrupt Enable Register (UART_IER)

Bit	Bit Name	Description	RW	InitVal
7-6		Reserved.		
5	ELP	Enable Low Power mode.	RW	0
3	EDSSI	Enable Modem Status Register Interrupt.	RW	0
4	ESLP	Enable Sleep mode.	RW	0
2	ELSI	Enable receiver Line Status Interrupt.	RW	0
1	ETBEI	Enable Transmitter holding register Empty Interrupt.	RW	0
0	ERDI	Enable Received Data available Interrupt.	RW	0

14.3. Interrupt Identification Register (UART_IIR)

Table 45. Interrupt Identification Register (UART_IIR)

Bit	Bit Name	Description	RW	InitVal
7:5	FIFO64[2:0]	000 = No FIFO 110 = 16-byte FIFO	R	110
4		Reserved.	R	0
3:1	IID[2:0]	Interrupt ID. IID[1:0] indicates the interrupt priority.	R	000
0	IPND	Interrupt Pending. 0: Interrupt pending	R	0

14.4. Interrupt Priority

Table 46. Interrupt Priority

Interrupt Identification Register				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
Bit3	Bit2	Bit1	Bit0				
0	0	0	1	None	None.	None.	None.
0	1	1	0	1	Receiver line status.	Overrun, parity, framing errors, or break.	Read LSR.
0	1	0	0	2	Received data available.	DR bit is set.	Read RBR.
1	1	0	0	2	Character time-out indication.	There is at least one character in the Rx FIFO and the Rx FIFO has not been read for a period of time (the time required to receive 4 characters).	Read RBR.
0	0	1	0	3	Transmitter holding register empty.	THRE bit set.	Read IIR or write THR.
0	0	0	0	4	Modem status.	CTS#, DSR#, RI#, DCD#.	Read MSR.

14.5. FIFO Control Register (UART_FCR)

Table 47. FIFO Control Register (UART_FCR)

Bit	Bit Name	Description	RW	InitVal
7-6	RTRG[1:0]	Receiver trigger level. Trigger level: 16-byte. 00 = 01 01 = 04 10 = 08 11 = 14	W	11
3-5		Reserved.		
2	TFRST	Transmitter FIFO Reset. Writes 1 to clear the transmitter FIFO buffer.	W	0
1	RFRST	Receiver FIFO Reset. Writes 1 to clear the receiver FIFO buffer.	W	0
0	EFIFO	Enable FIFO. When this bit is set, enables the transmitter and receiver FIFO buffers. Changing this bit clears the FIFOs.	W	0

14.6. Line Control Register (UART_LCR)

Table 48. Line Control Register (UART_LCR)

Bit	Bit Name	Description	RW	InitVal
7	DLAB	Divisor Latch Access Bit.	RW	0
6	BRK	Break control. Setting this bit forces TXD to the spacing (low) state (break). Clear this bit to disable the break condition.	RW	0
5-4	EPS[1:0]	Even Parity Select. 00 = Odd parity 01 = Even parity 10 = Mark parity 11 = Space parity	RW	0
3	PEN	Parity Enable.	RW	0
2	STB	Number of Stop Bits. 0: 1 bit 1: 2 bits	RW	0
1-0	WLS[1:0]	Word Length Select. 10: 7 bits 11: 8 bits	RW	11

14.7. Modem Control Register (UART_MCR)

Table 49. Modem Control Register (UART_MCR)

Bit	Bit Name	Description	RW	InitVal
7-6		Reserved.		
5	AFE	Auto Flow control Enable.	RW	0
4	LOOP	Loopback.	RW	0
2-3		Reserved.		
1	RTS	Request To Send. 0: Set RTS# high 1: Set RTS# low	RW	0
0		Reserved.		

14.8. Line Status Register (UART_LSR)

Table 50. Line Status Register (UART_LSR)

Bit	Bit Name	Description	RW	InitVal
7	RFE	Receive FIFO Errors. At least one parity, framing, or break error in the FIFO.	R	0
6	TEMT	Transmitter Empty. Character mode: Both THR and TSR are empty. FIFO mode: Both transmitter FIFO and TSR are empty.	R	0
5	THRE	Transmitter Holding Register Empty. Character mode: THR is empty. FIFO mode: Transmitter FIFO is empty.	R	0
4	BI	Break Interrupt indicator.	R	0
3	FE	Framing Error.	R	0
2	PE	Parity Error.	R	0
1	OE	Overrun Error. An overrun occurs when the receiver FIFO is full and the next character is completely received in the receiver shift register. An OE is indicated. The character in the shift register will be overwritten.	R	0
0	DR	Data Ready. Character mode: Data ready in RBR. FIFO mode: Receiver FIFO is not empty.	R	0

14.9. Modem Status Register (UART_MSR)

Table 51. Modem Status Register (UART_MSR)

Bit	Bit Name	Description	RW	InitVal
7	DCD	In loopback mode, returns bit 2 of MCR. In normal mode, returns 1.	R	1
6	RI	In loopback mode, returns bit 3 of MCR. In normal mode, returns 0.	R	0
5	DSR	In loopback mode, returns bit 0 of MCR In normal mode, returns 1.	R	1
4	CTS	Clear To Send. 0: CTS# detected high. 1: CTS# detected low.	R	0
3-1		Reserved.		
0	ΔCTS	Delta Clear To Send. CTS# signal transits.	R	0

15. Timer & Watchdog

There are four sets of hardware timers and one watchdog timer. Each timer can be configured as timer mode or counter mode. In both counter and timer mode, the time value is counted down from the initial value to zero (the value is reduced one for every timer clock). When configured as timer mode, the source of the timer clock can be the base clock, or based on the base clock divided by a configurable register value – CDBR: this is called a Basic timer. When the value reaches zero, the timer stops and an interrupt is issued.

When an interrupt is issued in timer mode, the time value will be reset to its initial value and the count down will restart. An interrupt will be issued whenever the count down value reaches zero.

When watchdog timer is enabled, it will cause a system reset when a time-out occurs. The time-out interval may be set in the registers. The time unit value is based on the base clock divided by the base value.

15.1. Timer & Watchdog Register Set

Table 52. Timer & Watchdog Register Set

Virtual Address	Size (byte)	Name	Description	Access
0xBD01_0050	2	TCCNR	Timer/Counter Control Register.	RW
0xBD01_0054	1	TCIR	Timer/Counter Interrupt Register.	RW
0xBD01_0058	1	CDBR	Clock Division Base Register.	RW
0xBD01_005C	2	WDTCNR	Watchdog Timer Control Register.	RW
0xBD01_0060	3	TC0DATA	Timer/Counter 0 Data register. Specifies the time-out duration.	RW
0xBD01_0064	3	TC1DATA	Timer/Counter 1 Data register. Specifies the time-out duration.	RW
0xBD01_0068	4	TC2DATA	Timer/Counter 2 Data register. Specifies the time-out duration.	RW
0xBD01_006C	4	TC3DATA	Timer/Counter 3 Data register. Specifies the time-out duration.	RW
0xBD01_0070	3	TC0CNT	Timer/Counter 0 Count register.	R
0xBD01_0074	3	TC1CNT	Timer/Counter 1 Count register.	R
0xBD01_0078	4	TC2CNT	Timer/Counter 2 Count register.	R
0xBD01_007C	4	TC3CNT	Timer/Counter 3 Count register.	R

15.2. Timer/Counter 0 Data Register (TC0CNT)

Table 53. Timer/Counter 0 Data Register (TC0CNT)

Bit	Bit Name	Description	RW	InitVal
23-0	TC0Value[23:0]	The Timer or Counter initial value.	RW	

15.3. Timer/Counter 1 Data Register (TC1CNT)

Table 54. Timer/Counter 1 Data Register (TC1CNT)

Bit	Bit Name	Description	RW	InitVal
23-0	TC1Value[23:0]	The Timer or Counter initial value.	RW	

15.4. Timer/Counter 2 Data Register (TC2CNT)

Table 55. Timer/Counter 2 Data Register (TC2CNT)

Bit	Bit Name	Description	RW	InitVal
31-0	TC2Value[31:0]	The Timer or Counter initial value.	RW	

15.5. Timer/Counter 3 Data Register (TC3CNT)

Table 56. Timer/Counter 3 Data Register (TC3CNT)

Bit	Bit Name	Description	RW	InitVal
31-0	TC3Value[31:0]	The Timer or Counter initial value.	RW	

15.6. Timer/Counter Control Register (TCCNR)

Table 57. Timer/Counter Control Register (TCCNR)

Bit	Bit Name	Description	RW	InitVal
11	TC3Src	Timer/Counter 3 clock Source. 0: Base clock 1: Basic timer	RW	0
10	TC2Src	Timer/Counter 2 clock Source. 0: Base clock 1: Basic timer	RW	0
9	TC1Src	Timer/Counter 1 clock Source. 0: Base clock 1: Basic timer	RW	0
8	TC0Src	Timer/Counter 0 clock Source. 0: Base clock 1: Basic timer	RW	0
7	TC3Mode	Timer/Counter 3 Mode. 0: Counter mode 1: Timer mode	RW	0
6	TC3En	Timer/Counter 3 Enable.	RW	0
5	TC2Mode	Timer/Counter 2 Mode. 0: Counter mode 1: Timer mode	RW	0
4	TC2En	Timer/Counter 2 Enable.	RW	0
3	TC1Mode	Timer/Counter 1 mode. 0: Counter mode 1: Timer mode	RW	0
2	TC1En	Timer/Counter 1: Enable.	RW	0
1	TC0Mode	Timer/Counter 0 Mode. 0: Counter mode 1: Timer mode	RW	0
0	TC0En	Timer/Counter 0 Enable.	RW	0

15.7. Timer/Counter Interrupt Register (TCIR)

Table 58. Timer/Counter Interrupt Register (TCIR)

Bit	Bit Name	Description	RW	InitVal
7	TC3IP	Timer/Counter 3 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
6	TC2IP	Timer/Counter 2 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
5	TC1IP	Timer/Counter 1 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
4	TC0IP	Timer/Counter 0 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
3	TC3IE	Timer/Counter 3 Interrupt Enable.	RW	0
2	TC2IE	Timer/Counter 2 Interrupt Enable.	RW	0
1	TC1IE	Timer/Counter 1 Interrupt Enable.	RW	0
0	TC0IE	Timer/Counter 0 Interrupt Enable.	RW	0

15.8. Clock Division Base Register (CDBR)

Table 59. Clock Division Base Register (CDBR)

Bit	Bit Name	Description	RW	InitVal
15-0	DivFactor	The Division Factor of the clock source. If the DivFactor is N, the watchdog timer is divided by N+1. This value cannot be 0 in timer or watchdog mode. The clock source is 22MHz.	RW	0

15.9. Watchdog Control Register (WDTCNR)

Table 60. Watchdog Control Register (WDTCNR)

Bit	Bit Name	Description	RW	InitVal
10-9	OVSEL[1:0]	Overflow Select. These bits specify the overflow condition when the watchdog timer counts to the value. 00 = 2^{13} 01 = 2^{14} 10 = 2^{15} 11 = 2^{16}	RW	00
8	WDTCLR	Watchdog Clear. Writes a 1 to clear the watchdog counter.	W	0
7-0	WDTE[7:0]	Watchdog Enable. When these bits are set to 0xA5, the watchdog timer stops. Any value other than 0xA5 enables the watchdog timer, and the system will be reset when the overflow signal occurs.	W	0xA5

16. General Purpose Input/Output (GPIO)

The RTL8181/RTL8181P provides two sets of GPIO pins – PortA and PortB. Each has 16 pins. Each GPIO pin can be configured as an input or output pin via register PA(B)DIR. Register PA(B)DATA may be used to control the signals (high or low) of the GPIO pins. As the GPIO pins may be shared with some peripheral pins, PA(B)CNR can control the attributes of the shared pins. PortB GPIO sets can be used to generate interrupts via PBIMR, and the interrupt status is shown in PBISR.

16.1. GPIO Register Set

Table 61. GPIO Register Set

Virtual address	Size (byte)	Name	Description	Access
0xBD01_0040	4	PABDIR	Port A/B Direction Register.	RW
0xBD01_0044	4	PABDATA	Port A/B Data register.	RW
0xBD01_0048	4	PBIMR	Port B Interrupt Mask Register.	RW
0xBD01_004C	4	PBISR	Port B Interrupt Register.	R

16.2. Port A, B Direction Register (PADIR, PBDIR)

Table 62. Port A, B Direction Register (PADIR, PBDIR)

Bit	Bit Name	Description	RW	InitVal
31-16	DRCA[15:0]	Pin Direction Configuration of Port A. 0: Configured as input pin 1: Configured as output pin	RW	00
15-0	DRCB[15:0]	Pin Direction Configuration of Port B. 0: Configured as input pin 1: Configured as output pin	RW	00

16.3. Port A, B DATA Register (PADATA, PBDATA)

Table 63. Port A, B DATA Register (PADATA, PBDATA)

Bit	Bit Name	Description	RW	InitVal
31-16	DATAA[15:0]	Pin Data of Port A.	RW	00
15-0	DATAB[15:0]	Pin Data of Port B.	RW	00

16.4. Port B Interrupt Mask Register (PBIMR)

Table 64. Port B Interrupt Mask Register (PBIMR)

Bit	Bit Name	Description	RW	InitVal
1-0	PB0IM[1:0]	PortB.0 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
3-2	PB1IM[1:0]	PortB.1 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
5-4	PB2IM[1:0]	PortB.2 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
7-6	PB3IM[1:0]	PortB.3 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
9-8	PB4IM[1:0]	PortB.4 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
11-10	PB5IM[1:0]	PortB.5 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
13:12	PB6IM[1:0]	PortB.6 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
15-14	PB7IM[1:0]	PortB.7 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
17-16	PB8IM[1:0]	PortB.8 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
19-18	PB9IM[1:0]	PortB.9 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00

Bit	Bit Name	Description	RW	InitVal
21-20	PB10IM[1:0]	PortB.10 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
23:22	PB11IM[1:0]	PortB.11 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
25-24	PB12IM[1:0]	PortB.12 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
27-26	PB13IM[1:0]	PortB.13 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
29-28	PB14IM[1:0]	PortB.14 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00
31-30	PB15IM[1:0]	PortB.15 Interrupt Mode. 00 = Disable interrupt 01 = Enable falling edge interrupt 10 = Enable rising edge interrupt 11 = Enable both falling or rising edge interrupt	RW	00

16.5. Port B Interrupt Status Register (PBISR)

Table 65. Port B Interrupt Status Register (PBISR)

Bit	Bit Name	Description	RW	InitVal
15-0	PBIP[15:0]	Port B Interrupt Pending status. Self clear after read.	R	00

17. 802.11b WLAN Controller

The RTL8181/RTL8181P integrates a wireless LAN MAC and a direct sequence spread spectrum baseband processor, and fully complies with IEEE 802.11 and IEEE 802.11b specifications.

The RTL8181/RTL8181P features on-board A/D and D/A converters for analog I and Q inputs and outputs. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are provided along with complementary code keying to provide a variety of data rates. Both receive and transmit Automatic Gain Control (AGC) functions obtain maximum performance in the analog portions of the transceiver. It also includes a built-in enhanced signal detector to alleviate severe multi-path effects. The target environment for 11Mbps is 125ns RMS delay spread. It also supports short preamble and antenna diversity. For security, the RTL8181/RTL8181P implements a high performance internal WEP engine supporting up to 104-bit WEP.

The WLAN controller is a DMA bus-master device and uses descriptor-based buffer structure for packet transmission and reception. These features greatly contribute to overall system performance by offloading much of the packet handling from the CPU.

The RTL818 provides various interfaces for external RF modules. Currently it interfaces with Intersil, RFMD, Philips, Maxim, and GCT RF modules.

17.1. WLAN Controller Register Set

Table 66. WLAN Controller Register Set

Virtual Address	Size (byte)	Name	Description	RW
0xBD40_0000	8	WLAN_ID	ID Register. The ID register is only permitted to write via 4-byte access. Read access can be byte, word, or double word access.	RW
0xBD40_0008	8	WLAN_MAR	Multicast Register. The MAR register is only permitted to write via 4-byte access. Read access can be byte, word, or double word access.	RW
0xBD40_0018	8	WLAN_TSFTR	Timing Synchronization Function Timer Register.	R
0xBD40_0020	4	WLAN_TLPDA	Transmit Low Priority Descriptors Start Address (32-bit) (256-byte alignment).	RW
0xBD40_0024	4	WLAN_TNPDA	Transmit Normal Priority Descriptors Start Address (32-bit). (256-byte alignment).	RW
0xBD40_0028	4	WLAN_THPDA	Transmit High Priority Descriptors Start Address (32-bit). (256-byte alignment).	RW
0xBD40_002C	4	WLAN_BRSR	Basic Rate Set Register.	RW
0xBD40_002E	6	WLAN_BSSID	Basic Service Set ID.	RW
0xBD40_0037	1	WLAN_CR	Command Register.	RW
0xBD40_003C	2	WLAN_IMR	Interrupt Mask Register.	RW
0xBD40_003E	2	WLAN_ISR	Interrupt Status Register.	RW
0xBD40_0040	4	WLAN_TCR	Transmit (Tx) Configuration Register.	RW
0xBD40_0044	4	WLAN_RCR	Receive (Rx) Configuration Register.	RW

Virtual Address	Size (byte)	Name	Description	RW
0xBD40_0048	4	WLAN_TINT	Timer Interrupt Register. Once having written a non-zero value to this register, the Timeout bit of the WLAN_ISR register will be set whenever the least 32 bits of the WLAN_TSFTR reaches this value. The Timeout bit will not be set as long as the WLAN_TINT register is zero.	RW
0xBD40_004C	4	WLAN_TBDA	Transmit Beacon Descriptor start Address (32-bit) (256-byte alignment).	RW
0xBD40_0050	1	WLAN_CR	Command Register.	RW
0xBD40_0051	1	WLAN_CONFIG0	Configuration Register 0.	R
0xBD40_0053	1	WLAN_CONFIG2	Configuration Register 2.	RW
0xBD40_0054	4	WLAN_ANAPARM	Analog Parameter.	RW
0xBD40_0058	1	WLAN_MSR	Media Status Register.	RW
0xBD40_0059	1	WLAN_CONFIG3	Configuration Register 3.	RW
0xBD40_005A	1	WLAN_CONFIG4	Configuration Register 4.	RW
0xBD40_005B	1	WLAN_TESTR	Test mode Register.	RW
0xBD40_005F	1	WLAN_SCR	Security Configuration Register.	RW
0xBD40_0070	2	WLAN_BCNITV	Beacon Interval Register.	RW
0xBD40_0072	2	WLAN_ATIMWND	Atim Window Register.	RW
0xBD40_0074	2	WLAN_BINTRITV	Beacon interrupt Interval Register.	RW
0xBD40_0078	1	WLAN_PHYDELAY	PHY Delay Register.	RW
0xBD40_007A	2	WLAN_CRC16ERR	PLCP header CRC16 Error count.	RW
0xBD40_007C	1	WLAN_PHYADDR	PHY interface Address Register.	RW
0xBD40_007D	1	WLAN_PHYDATAW	Write Data to PHY.	W
0xBD40_007E	1	WLAN_PHYDATAR	Read Data from PHY.	R
0xBD40_0080	4	WLAN_PHYCFG	PHY Configuration register.	RW
0xBD40_0090	16	WLAN_DK0	WEP Default Key 0 register.	RW
0xBD40_00A0	16	WLAN_DK1	WEP Default Key 1 register.	RW
0xBD40_00B0	16	WLAN_DK2	WEP Default Key 2 register.	RW
0xBD40_00C0	16	WLAN_DK3	WEP Default Key 3 register.	RW
0xBD40_00D8	1	WLAN_ CONFIG5	Configuration Register 5.	RW
0xBD40_00D9	1	WLAN_TPPOLL	Transmit Priority Polling register.	W
0xBD40_00DC	2	WLAN_ CWR	Contention Window Register.	R
0xBD40_00DE	1	WLAN_RETRYCTR	Retry Count Register.	R
0xBD40_00E4	4	WLAN_RDSAR	Receive Descriptor Start Address Register (32-bit). (256-byte alignment).	RW
0xBD40_0100	6	WLAN_KMAR	Key Map MAC Address.	RW
0xBD40_0106	15	WLAN_KMKEY	Key Map Key Value.	RW
0xBD40_0116	2	WLAN_KMC	Key Map Config.	RW

17.2. TSF Timer Register (WLAN_TSFTR)

Table 67. TSF Timer Register (WLAN_TSFTR)

Bit	Bit Name	Description	RW
63-0	TSFT	Timing Synchronization Function Timer. The RTL8181/RTL8181P maintains a TSF timer with modules 2^64 counting in increments of microseconds. The 8 octets are the timestamp field of beacon and probe response frames.	R

17.3. Basic Rate Set Register (WLAN_BRSR)

Table 68. Basic Rate Set Register (WLAN_BRSR)

Bit	Bit Name	Description
15-9		Reserved.
8	BPLCP	Basic Physical Layer Convergence Protocol. 0: Long PLCP header for CTS/ACK packet. 1: Short PLCP header for CTS/ACK packet.
7-4		Reserved.
3-0	MBR	Basic Rate Set. All control frames shall be transmitted at the rate that is less than or equal to this setting. bit0: 1M, bit1: 2M, bit2: 5.5M, bit3: 11M

17.4. Basic Service Set ID Register (WLAN_BSSID)

Table 69. Basic Service Set ID Register (WLAN_BSSID)

Bit	Bit Name	Description	RW
47-0	BSSID	Basic Service Set Identification. This register is written to by the driver after a NIC joins a network or creates an ad-hoc network.	RW

17.5. Command Register (WLAN_CR)

This register is used for issuing commands to the WLAN controller. These commands are issued by setting the corresponding bits for the function. A global software reset along with individual reset and enable/disable for transmitter and receiver are provided here.

Table 70. Command Register (WLAN_CR)

Bit	Bit Name	Description	RW
7:5		Reserved.	
4	RST	Reset. Setting this bit to 1 forces the RTL8181/RTL8181P perform a WLAN MAC reset. During the reset state, it disables the transmitter and receiver and reinitializes the FIFOs. The values of WLAN_IDR and WLAN_MAR are not changed. This bit is 1 during the reset operation, and is cleared to 0 when the reset operation is complete.	RW
3	RE	Receiver Enable. When set to 1 whilst the receive state machine is idle, the receive machine becomes active. This bit will read back as 1 whenever the receive state machine is active. After initial power-up, software must insure that the receiver has completely reset before setting this bit. 1: Enable 0: Disable	RW
2	TE	Transmitter Enable. When set to 1 whilst the transmit state machine is idle, the transmit state machine becomes active. This bit will read back as 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit. 1: Enable 0: Disable	RW
1-0		Reserved.	

17.6. Interrupt Mask Register (WLAN_IMR)

This register masks the interrupts that can be generated from the Interrupt Status Register. A hardware reset will clear all mask bits. Setting a mask bit allows the corresponding bit in the Interrupt Status Register to cause an interrupt. The Interrupt Status Register bits are always set to 1 if the condition is present, regardless of the state of the corresponding mask bit.

Table 71. Interrupt Mask Register (WLAN_IMR)

Bit	Bit Name	Description	RW
15	TXFOVW	Tx FIFO Overflow Interrupt. 1: Enable 0: Disable	RW
14	TimeOut	Time Out interrupt. 1: Enable 0: Disable	RW
13	BcnInt	Beacon Time out Interrupt. 1: Enable 0: Disable	RW
12	ATIMInt	ATIM Time Out Interrupt. 1: Enable 0: Disable	RW
11	TBDER	Tx Beacon Descriptor Error interrupt. 1: Enable 0: Disable	RW
10	TBDOK	Tx Beacon Descriptor OK interrupt. 1: Enable 0: Disable	RW
9	THPDER	Tx High Priority Descriptor Error interrupt. 1: Enable 0: Disable	RW
8	THPDOK	Tx High Priority Descriptor OK interrupt. 1: Enable 0: Disable	RW
7	TNPDER	Tx Normal Priority Descriptor Error interrupt. 1: Enable 0: Disable	RW
6	TNPDOK	Tx Normal Priority Descriptor OK interrupt. 1: Enable 0: Disable	RW
5	RXFOVW	Rx FIFO Overflow interrupt. 1: Enable 0: Disable	RW
4	RDU	Rx Descriptor Unavailable interrupt. 1: Enable 0: Disable	RW
3	TLPDER	Tx Low Priority Descriptor Error interrupt. 1: Enable 0: Disable	RW
2	TLPDOK	Tx Low Priority Descriptor OK interrupt. 1: Enable 0: Disable	RW

Bit	Bit Name	Description	RW
1	RER	Rx Error interrupt. 1: Enable 0: Disable	RW
0	ROK	Rx OK interrupt. 1: Enable 0: Disable	RW

17.7. Interrupt Status Register (WLAN_ISR)

This register indicates the source of a WLAN controller interrupt. Enabling the corresponding bits in the Interrupt Mask Register (WLAN_IMR) allows bits in this register to produce an interrupt. When an interrupt is active, one of more bits in this register are set to a 1. The interrupt Status Register reflects all current pending interrupts, regardless of the state of the corresponding mask bit in the WLAN_IMR. Reading the WLAN_ISR clears all interrupts. Writing a 1 to any bit in this register will reset that bit.

Table 72. Interrupt Status Register (WLAN_ISR)

Bit	Symbol	Description	RW
15	TXFOVW	Tx FIFO Overflow.	RW
14	TimeOut	Time Out. This bit is set to 1 when the least 32 bits of the TSFTR register reaches the value of the TimerInt register.	RW
13	BcnInt	Beacon time out Interrupt. When set, this bit indicates that the TBTT (Target Beacon Transmission Time) has reached the value set in the Beacon Interrupt Interval Register.	RW
12	ATIMInt	ATIM Time Out Interrupt. When set, this bit indicates that the ATIM window has reached the value set in the Atim Interrupt Interval Register.	RW
11	TBDER	Transmit Beacon priority Descriptor Error. Indicates that a beacon priority descriptor transmission was aborted due to reception of a beacon frame.	RW
10	TBDOK	Transmit Beacon priority Descriptor OK. Indicates that a beacon priority descriptor exchange sequence has been successfully completed.	RW
9	THPDER	Transmit High Priority Descriptor Error. Indicates that a high priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) having reached SRL (Short Retry Limit), or an SLRC (Station Long Retry Count) having reached LRL (Long Retry Limit).	RW
8	THPDOK	Transmit High Priority Descriptor OK. Indicates that a high priority descriptor exchange sequence has been successfully completed.	RW
7	TNPDER	Transmit Normal Priority Descriptor Error. Indicates that a normal priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) having reached SRL (Short Retry Limit), or an SLRC (Station Long Retry Count) having reached LRL (Long Retry Limit).	RW
6	TNPDOK	Transmit Normal Priority Descriptor OK. Indicates that a normal priority descriptor exchange sequence has been successfully completed.	RW
5	FOVW	Rx FIFO Overflow. This bit set to 1 is caused by Receive Descriptor Unavailable (RDU), poor PCI performance, or overloaded PCI traffic.	RW
4	_RDU	Rx Descriptor Unavailable. When set, this bit indicates that the Rx descriptor is currently unavailable.	RW

Bit	Symbol	Description	RW
3	TLPDER	Transmit Low Priority Descriptor Error. Indicates that a low priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) having reached SRL (Short Retry Limit), or an SLRC (Station Long Retry Count) having reached LRL (Long Retry Limit).	RW
2	TLPDOK	Transmit Low Priority Descriptor OK. Indicates that a low priority descriptor exchange sequence has been successfully completed.	RW
1	RER	Receive Error. Indicates that a packet has a CRC32 or ICV error.	RW
0	ROK	Receive OK. In normal mode, indicates the successful completion of a packet reception.	RW

17.8. Transmit Configuration Register (WLAN_TCR)

This register defines the Transmit Configuration for the WLAN controller. It controls such functions as loopback, heartbeat, auto-transmit padding, programmable InterFrame Gap, fill and drain thresholds, and maximum DMA burst size.

Table 73. Transmit Configuration Register (WLAN_TCR)

Bit	Symbol	Description	RW
31	CWMIN	Contention Window Minimum value. Set to 1 to indicate that Cwmin=8. Set to 0 to indicate that Cwmin=32.	RW
30	SEQGEN	Sequence number Generation switch. 0: Enabled. Sequence number is generated by the RTL8181/RTL8181P 1: Disabled. Sequence number should be generated by software	
29-25		Reserved.	
24	SAT	Set ACK Timeout. The EIFS, ACK, and CTS timeouts are derived from the following equation: EIFS = 112/ACKrate + 252 0: ACKrate is fixed at 1Mbps 1: ACKrate is dependent on the higher of MBR (bits 1:0, BRSR) and Rx DATA/RTS rate	RW
23-21	MXDMA2, 1, 0	Max DMA burst size per Tx DMA burst. This field sets the maximum size of transmit DMA data bursts according to the following: 000: 16 bytes, 001: 32 bytes, 010: 64 bytes, 011: 128 bytes, 100: 256 bytes, 101: 512 bytes, 110: 1024 bytes, 111: 2048 bytes	RW
20	DISCW	Disable Contention Window Backoff. This bit indicates the existence of a backoff procedure during packet transmission. 0: Uses IEEE 802.11 random backoff procedure 1: No random backoff procedure	RW
19	ICV	Append ICV (Integrity Check Value). This bit indicates the existence of an ICV appended at the end of an encipherment packet. 0: ICV appended 1: No ICV appended	RW
18-17	LBK1, LBK0	Loopback Test. There are no packets on the TXI+/- and TXQ+/- lines under the Loopback test condition. The loopback function must be independent of the link state. 00: Normal operation, 01: MAC Loopback 10: Baseband Loopback, 11: Continue TX.	RW

Bit	Symbol	Description	RW
16	CRC	Append CRC32. This bit indicates the existence of a CRC32 appended at the end of a packet. 0: A CRC32 is appended 1: No CRC32 appended	RW
15-8	SRL	Short Retry Limit RTS Retry Limit. Indicates the maximum retry time for frames of length less than or equal to the RTSThreshold.	RW
7-0	LRL	Long Retry Limit: Data Packet Retry Limit. Indicates the maximum retransmission times for Data or Management frames of length greater than RTSThreshold.	RW

17.9. Receive Configuration Register (WLAN_RCR)

This register is used to set the receive configuration for the WLAN controller. Receive properties such as accepting error packets, runt packets, setting the receive drain threshold etc. are controlled here.

Table 74. Receive Configuration Register (WLAN_RCR)

Bit	Bit Name	Description	RW
31	ONLYERLPKT	Early Receiving based on Packet Size. Early Receiving is only performed for packets with a size greater than 1536 bytes.	RW
30	ENCS2	Enable Carrier Sense Detection Method 2.	RW
29	ENCS1	Enable Carrier Sense Detection Method 1.	RW
28	ENMARP	Enable MAC Auto-reset PHY.	RW
27-24		Reserved.	
23	CBSSID	Check BSSID ‘To DS’ and ‘From DS’ Match Packet. When set to 1, the RTL8181/RTL8181P will check the Rx data type frame’s BSSID ‘To DS’ and ‘From DS’ fields, according to NETYPE (bits 3:2, MSR), to determine if it is set to Link ok.	RW
22	APWRMGT	Accept Power Management packet. This bit determines whether the RTL8181/RTL8181P will accept or reject packets with the power management bit set. 0: Reject 1: Accept	RW
21	ADD3	Accept Address 3 match packets. Set this bit to 1 to accept broadcast/multicast data type frames that Address 3 match the RTL8181/RTL8181P’s MAC address. This bit is valid only when NETYPE (bits 3:2, MSR) is set to Link ok in an Infrastructure network.	RW
20	AMF	Accept Management Frame. This bit determines whether the RTL8181/RTL8181P will accept or reject a management frame. 0: Reject 1: Accept	RW
19	ACF	Accept Control Frame. This bit determines whether the RTL8181/RTL8181P will accept or reject a control frame. 0: Reject 1: Accept	RW
18	ADF	Accept Data Frame. This bit determines whether the RTL8181/RTL8181P will accept or reject a data frame. 0: Reject 1: Accept	RW

Bit	Bit Name	Description	RW
17-16		Reserved.	
15-13	RXFTH2, 1, 0	Rx FIFO Threshold. This bit specifies the Rx FIFO Threshold level. When the number of the received data bytes from a packet being received into the Rx FIFO of the RTL8181/RTL8181P has reached the set level (or the FIFO contains a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following: 000: Reserved, 001: Reserved, 010: 64 bytes, 011: 128 bytes 100: 256 bytes, 101: 512 bytes, 110: 1024 bytes, 111: No Rx threshold. The RTL8181/RTL8181P begins the transfer of data after receiving a whole packet into the FIFO.	
12	AICV	Accept ICV error packets. This bit determines whether packets with ICV (Integrity Check Value) errors will be accepted or rejected. 1: Accept 0: Reject	
11		Reserved.	
10-8	MXDMA2, 1, 0	Max. DMA burst size per Rx DMA burst. This field sets the maximum size of the receive DMA data bursts according to the following: 000: 16 bytes, 001: 32 bytes, 010: 64 bytes, 011: 128 bytes 100: 256 bytes, 101: 512 bytes, 110: 1024 bytes, 111: Unlimited	
7-6		Reserved.	
5	ACRC32	Accept CRC32 error packets. This bit determines whether packets with CRC32 errors will be accepted or rejected. 0: Reject 1: Accept	
4		Reserved.	
3	AB	Accept Broadcast packets. This bit determines whether broadcast packets will be accepted or rejected. 0: Reject 1: Accept	
2	AM	Accept Multicast packets. This bit determines whether multicast packets will be accepted or rejected. 0: Reject 1: Accept	
1	APM	Accept Physical Match packets. This bit determines whether physical match packets will be accepted or rejected. 0: Reject 1: Accept	
0	AAP	Accept destination Address Packets. This bit determines whether packets with a destination address will be accepted or rejected. 0: Reject 1: Accept	

17.10. Command Register (WLAN_CR)

This register is used for issuing commands to the WLAN controller. These commands are issued by setting the corresponding bits for the function. A warm software reset along with individual reset and enable/disable for transmitter and receiver are also provided.

Table 75. Command Register (WLAN_CR)

Bit	Bit Name	Description	RW
7-6	EEM	These 2 bits select the operating mode. 00: Operating in network/host communication mode. 11: Before writing to the WLAN_CONFIG0, 1, 2, and 3 registers, the RTL8181/RTL8181P must be placed in this mode. This prevents accidental changes to the WLAN controller configurations.	RW
5-0		Reserved.	

17.11. Configuration Register 0 (WLAN_CONFIG0)

Table 76. Configuration Register 0 (WLAN_CONFIG0)

Bit	Bit Name	Description	RW
7-4		Reserved.	
3	Aux_Status	Auxiliary power present Status. This bit indicates the existence of auxiliary power. The value of this bit is fixed after each reset. 1: Auxiliary power is present 0: Auxiliary power is absent	RW
2		Reserved.	
1-0	GL	Geographic Location. These bits indicate the current operational region in which the RTL8181/RTL8181P transmits and receives packets. 11: USA, 10: Europe, 0: Japan	RW

17.12. Configuration Register 2 (WLAN_CONFIG2)

Table 77. Configuration Register 2 (WLAN_CONFIG2)

Bit	Bit Name	Description	RW
7	LCK	Locked Clocks. Set this bit to 1 to lock the transmit frequency and symbol clocks to the same oscillator.	RW
6	ANT	Antenna diversity. 0: Disable 1: Enable	RW
5-4		Reserved.	
3	DPS	Descriptor Polling State. Test mode. 0: Normal working state. This is also the power-on default value 1: Test mode	RW
2	PAPE_sign	Power Amplifier Enable timing. 1: The RTL8181/RTL8181P will advance PAPE_time to enable the PAPE pin when transmitting data 0: The RTL8181/RTL8181P will delay PAPE_time to enable the PAPE pin when transmitting data	RW
1-0	PAPE_time	These two bits indicate that the RTL8181/RTL8181P has enabled the PAPE pin (in µs).	RW

17.13. Media Status Register (WLAN_MSR)

This register allows configuration of device and PHY options, and provides PHY status information.

Table 78. Media Status Register (WLAN_MSR)

Bit	Bit Name	Description	RW
7-4		Reserved.	
3-2	NETTYPE	Network Type and Link Status. The values of these bits are written by the driver. 10: Infrastructure client, 01: Ad-hoc, 11: Access Point, 00: No link	RW
1-0		Reserved.	

17.14. Configuration Register 3 (WLAN_CONFIG3)

Table 79. Configuration Register 3 (WLAN_CONFIG3)

Bit	Bit Name	Description	RW
7		Reserved.	
6	PARM_En	Parameter write Enable. Setting this bit to 1 and asserting WLAN_CR register bit EEM1 and EEM0 at the same time will enable the WLAN_ANAPARM register to be written via software.	RW
4-1		Reserved.	
0	FBtBEn	Fast Back to Back Enable. 0: Disable 1: Enable	RW

17.15. Configuration Register 4 (WLAN_CONFIG4)

Table 80. Configuration Register 4 (WLAN_CONFIG4)

Bit	Bit Name	Description	RW
7	VCOPDN	VCO Power Down. 0: Normal working state. This is the power-on default value 1: VCO power down mode. Setting this bit enables the VCOPDN pin and turns off the external RF front end power (including VCO) and most of the internal power of the RTL8181/RTL8181P	RW
6	PWROFF	Power Off. 0: Normal working state. This is the power-on default value 1: Power Off mode. Turn off the external RF front end power (excluding VCO) and most of the internal power of the RTL8181/RTL8181P	RW
5	PWRMGT	Power Management. 0: Normal working state. This is the power-on default value 1: Power management mode. Sets a Tx packet's power management bit to 1 to include a control type frame	RW
4-2		Reserved.	
1-0	RFTYPE	RF module Type. The combination of these two bits indicate the type of RF module being used with the RTL8181/RTL8181P. 11: Philips, 10: RFMD, 01: Intersil	RW

17.16. Security Configuration Register (WLAN_SCR)

Table 81. Security Configuration Register (WLAN_SCR)

Bit	Bit Name	Description	RW
7-6		Reserved.	
5-4	KM	Key Mode. The combination of these two bits sets the type of security scheme to use. 00: WEP40, 01: WEP104	RW
3-2		Reserved.	
1	TXSECON	TX Security ON. Set this bit to 1 to turn on the optional Tx path security scheme. This bit is written by software and is invalid when WEP40 (bit7, WLAN_CONFIG0), and WEP104 (bit6, WLAN_CONFIG0) are set to 0.	RW
0	RXSECON	RX Security ON. Set this bit to 1 to turn on the optional Rx path security scheme. This bit is written by software and is invalid when WEP40 (bit7, WLAN_CONFIG0), and WEP104 (bit6, WLAN_CONFIG0) are set to 0.	RW

17.17. Beacon Interval Register (WLAN_BCNITV)

Table 82. Beacon Interval Register (WLAN_BCNITV)

Bit	Bit Name	Description	RW
15-10		Reserved.	
9-0	BcnItv	Beacon Interval. The Beacon Interval represents the number of time units (1 TU = 1024μs) between target beacon transmissions (TBTTs). This register is written by the driver after starting a BSS/IBSS or joining an IBSS network.	RW

17.18. ATIM Window Register (WLAN_ATIMWND)

Table 83. ATIM Window Register (WLAN_ATIMWND)

Bit	Bit Name	Description	RW
15-10		Reserved.	
9-0	AtimWnd	This register indicates the ATIM Window length in Time Units (TU). It is written by the driver after the NIC joins or creates an ad-hoc network.	RW

17.19. Beacon Interrupt Interval Register (WLAN_BINTRITV)

Table 84. Beacon Interrupt Interval Register (WLAN_BINTRITV)

Bit	Bit Name	Description	RW
15-10		Reserved.	
9-0	BintrItv	This timer register generates BcnInt (bit 13, ISR) at a set time interval before TBTT to prompt the host to prepare the beacon. The unit of this register is microseconds. It is written by the driver after the NIC joins a network or creates an ad-hoc network.	RW

17.20. Atim Interrupt Interval Register (WLAN_ATIMTRITV)

Table 85. ATIM Interrupt Interval Register (WLAN_ATIMTRITV)

Bit	Bit Name	Description	RW
15-10		Reserved.	
9-0	AtimtrItv	This timer register generates ATIMInt (bit 12, ISR) at a set time interval before the end of the ATIM window in an ad-hoc network. The unit of this register is microseconds. It is written by the driver after the NIC joins a network or creates an ad-hoc network.	RW

17.21. PHY Delay Register (WLAN_PHYDELAY)

Table 86. PHY Delay Register (WLAN_PHYDELAY)

Bit	Bit Name	Description	RW
7-3		Reserved.	
2-0	PhyDelay	Physical layer Delay. These three bits represent the delay time in μs between the MAC and RF front end when transmitting data.	RW

17.22. Default Key 0 Register (WLAN_DK0)

Table 87. Default Key 0 Register (WLAN_DK0)

Bit	Bit Name	Description	RW
127-104		Reserved.	
103-0	DK0	Default Key 0. When WEP104 is configured in the set KM register, bits 0-103 will contain the 104-bit WEP key value for default key 0. If WEP40 is set, bits 0-39 will contain the 40-bit WEP key value for default key 0. This register may only be read/written via 4-byte access.	RW

17.23. Default Key 1 Register (WLAN_DK1)

Table 88. Default Key 1 Register (WLAN_DK1)

Bit	Bit Name	Description	RW
127-104		Reserved.	
103-0	DK1	Default Key 1. When WEP104 is configured in the set KM register, bits 0-103 will contain the 104-bit WEP key value for default key 1. If WEP40 is set, bits 0-39 will contain the 40-bit WEP key value for default key 1. This register may only be read/written via 4-byte access.	RW

17.24. Default Key 2 Register (WLAN_DK2)

Table 89. Default Key 2 Register (WLAN_DK2)

Bit	Bit Name	Description	RW
127-104		Reserved.	
103:0	DK2	Default Key 2. When WEP104 is configured in the set KM register, bits 0-103 will contain the 104-bit WEP key value for default key 2. If WEP40 is set, bits 0-39 will contain the 40-bit WEP key value for default key 2. This register may only be read/written via 4-byte access.	RW

17.25. Default Key 3 Register (WLAN_DK3)

Table 90. Default Key 3 Register (WLAN_DK3)

Bit	Bit Name	Description	RW
127-104		Reserved.	
103-0	DK3	Default Key 3. When WEP104 is configured in the set KM register, bits 0-103 will contain the 104-bit WEP key value for default key 3. If WEP40 is set, bits 0-39 will contain the 40-bit WEP key value for default key 3. This register may only be read/written via 4-byte access.	RW

17.26. Configuration Register 5 (WLAN_CONFIG5)

This register, unlike other Configuration registers, is not protected by the Command register. There is no need to enable the Config register write prior to writing to Config5.

Table 91. Configuration Register 5 (WLAN_CONFIG5)

Bit	Bit Name	Description	RW
7	TX_FIFO_OK	Built in self-test for TX FIFO. 0: Fail 1: OK	R
6	RX_FIFO_OK	Built in self-test for RX FIFO. 0: Fail 1: OK	R
5	CALON	Calibration ON. 0: Put the AGCRESET pin to ground 1: Activate the calibration cycle, and hold the AGCRESET pin high	RW
4-0		Reserved.	

17.27. Transmit Priority Polling Register (WLAN_TPPOLL)

Table 92. Transmit Priority Polling Register (WLAN_TPPOLL)

Bit	Bit Name	Description	RW
7	BQ	Beacon Queue polling. The RTL8181/RTL8181P will clear this bit automatically after a beacon packet has been transmitted or received. Writing to this bit has no effect.	W
6	HPQ	High Priority Queue polling. Write a 1 to this bit by software to notify the RTL8181/RTL8181P that there is a high priority packet waiting to be transmitted. The RTL8181/RTL8181P will clear this bit automatically after all high priority packets have been transmitted. Writing a 0 to this bit has no effect.	W
5	NPQ	Normal Priority Queue polling. DPS (bit3, Config 2) set to 0: The RTL8181/RTL8181P will clear this bit automatically after all normal priority packets have been transmitted or received. Writing to this bit has no effect. DPS (bit3, Config 2) set to 1: Write a 1 to this bit via software to notify the RTL8181/RTL8181P that there is a normal priority packet waiting to be transmitted. The RTL8181/RTL8181P will clear this bit automatically after all normal priority packets have been transmitted. Writing a 0 to this bit has no effect.	W
4	LPQ	Low Priority Queue polling. Write a 1 to this bit via software to notify the RTL8181/RTL8181P that there is a low priority packet(s) waiting to be transmitted. The RTL8181/RTL8181P will clear this bit automatically after all low priority packets have been transmitted. Writing a 0 to this bit has no effect.	W
3	SBQ	Stop Beacon Queue. Write a 1 to this bit via software to notify the RTL8181/RTL8181P to stop the DMA mechanism of the Beacon Queue. This bit is invalid when DPS (bit3, Config 2) is set to 1.	W
2	SHPQ	Stop High Priority Queue. Write a 1 to this bit via software to notify the RTL8181/RTL8181P to stop the DMA mechanism of the High Priority Queue.	W
1	SNPQ	Stop Normal Priority Queue. Write a 1 to this bit via software to notify the RTL8181/RTL8181P to stop the DMA mechanism of the Normal Priority Queue. This bit is invalid when DPS (bit3, Config 2) is set to 1.	W
0	SLPQ	Stop Low Priority Queue. Write a 1 to this bit via software to notify the RTL8181/RTL8181P to stop the DMA mechanism of the Low Priority Queue.	W

17.28. Contention Window Register (WLAN_CWR)

Table 93. Contention Window Register (WLAN_CWR)

Bit	Bit Name	Description	RW
15-10		Reserved.	
9-0	CW	Contention Window. This register indicates the number of contention windows before transmitting a packet.	R

17.29. Retry Count Register (WLAN_RETRYCTR)

Table 94. Retry Count Register (WLAN_RETRYCTR)

Bit	Bit Name	Description	RW
7-0	RetryCT	Retry Count. This register indicates the number of retry counts when a packet transmission has completed.	R

17.30. Receive Descriptor Start Address Reg. (WLAN_RDSAR)

Table 95. Receive Descriptor Start Address Register (WLAN_RDSAR)

Bit	Bit Name	Description	RW
31-0	RDSA	Receive Descriptor Start Address. This is a 32-bit address.	RW

18. WEP Key Mapping

The WEP key table contains 64 entries that include the key to be used to encrypt the transmit packets and decrypt received packets. Each entry contains the MAC address, associated key value, key type (40-bits or 104-bits) and a key-valid flag.

The table cannot be accessed directly. To set/get an entry to/from the table, you must go through registers because the key table is embedded in the ASIC. When reading/writing an entry, you must specify which table entry you are going to access via an index value defined in register KeyMapIdx.

For example, to update a table entry, you need to set the MAC address in keyMapAddr, set the key value in KeyMapKey, specify the key type (40-bits or 104-bits) in KeyMapType, set the table index in keyMapIdx, assert the valid flag in KeyMapValid, and write '1' in KeyMapOp as a 'write' operation. After setting these values, set '1' in the register KeyMapPoll bit to tell the WLAN controller to process the request. Wait for the WLAN controller to accomplish the operation by polling the KeyMapPoll bit until it is cleared.

There is no default value for these registers in initialization. You must reset the KeyMapValid flag for those entries not used.

18.1. Key Map MAC Address (WLAN_KMAR)

Table 96. Key Map MAC Address (WLAN_KMAR)

Bit	Bit Name	Description	RW
47-0	KeyMapAddr	MAC address.	RW

18.2. Key Map Key Value (WLAN_KMKEY)

Table 97. Key Map Key Value (WLAN_KMKEY)

Bit	Bit Name	Description	RW
127-0	KeyMapKey	WEP key value.	RW

18.3. Key Map Config (WLAN_KMC)

Table 98. Key Map Config (WLAN_KMC)

Bit	Bit Name	Description	RW
15-10	KeyMapIdx	Key Map Index. Specifies the table entry to read or write.	RW
9-8	KeyMapType	Key value Type. 0: 40-bit, 1: 104-bit, 2: Reserved, 3: Reserved	RW
7	KeyMapValid	Valid flag. If this bit is '1', it indicates the table entry indexed by KeyMapIdx, is valid. Bit '0' implies the entry is invalid.	RW
6	KeyMapOp	Operation for writing or reading key value. Value '1' indicates to set a key value, '0' means to get a key value.	RW
5	KeyMapPoll	Polling bit of read/write key. Set to '1' to make the RTL8181/RTL8181P begin to read/write the value of the key table whose entry index is specified in *KeyMapIdx*. The RTL8181/RTL8181P will clear the bit automatically after the operation has completed. Writing '0' to this bit has no effect.	RW
4-0		Reserved.	

19. Packet Buffering

The RTL8181/RTL8181P WLAN controller incorporates two independent FIFO buffers for transferring data to/from the system interface and from/to the network. The FIFOs provide temporary storage of data, freeing the host system from the real-time demands of the network.

The way in which the FIFOs are emptied and filled is controlled by the FIFO threshold values in the Receive Configuration registers. These values determine how full or empty the FIFOs must be before the device requests the bus. Once the RTL8181/RTL8181P requests the bus, it will attempt to empty or fill the FIFOs as allowed by the respective MXDMA settings in the Transmit Configuration and Receive Configuration registers.

19.1. Transmit Buffer Manager

The buffer management scheme used on the WLAN controller allows quick, simple, and efficient use of the frame buffer memory. The buffer management scheme uses separate buffers and descriptors for packet information. This allows effective transfers of data to the transmit buffer manager by simply transferring the descriptor information to the transmit queue.

The Tx Buffer Manager DMAs packet data from system memory and places it in the 4KB transmit FIFO, and pulls data from the FIFO to send to the Tx MAC. Multiple packets may be present in the FIFO, allowing packets to be transmitted with short inter-frame spaces. Additionally, once the RTL8181/RTL8181P requests the bus, it will attempt to fill the FIFO as allowed by the MXDMA setting.

The Tx Buffer Manager process also supports priority queuing of transmit packets. It handles this by drawing from two separate descriptor lists to fill the internal FIFO. If packets are available in the high priority queues, they will be loaded into the FIFO before those of low priority.

19.2. Receive Buffer Manager

The Rx Buffer Manager uses the same buffer management scheme as used for transmits. The Rx Buffer Manager retrieves packet data from the Rx MAC and places it in the 2KB receive data FIFO, and pulls data from the FIFO for DMA to system memory. The receive FIFO is controlled by the FIFO threshold value in RXFTH. This value determines the number of long words written into the FIFO from the MAC unit before a DMA request for system memory occurs. Once the RTL8181/RTL8181P gets the bus, it will continue to transfer the long words from the FIFO until the data in the FIFO is less than one long word, or has reached the end of the packet, or the max DMA burst size is reached, as set in MXDMA.

20. Characteristics

20.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltage are specified reference to GND unless otherwise specified.

Table 99. Electrical Characteristics/Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Vcc Supply Referenced to GND	-0.5	+4.0	V
Digital Input Voltage	-0.5	VDD	V
DC Output Voltage	-0.5	VDD	V

20.2. Operating Range

Parameter	Min	Max	Units
Ambient Operating Temperature	0	+70	°C
3.3 Vcc Supply Voltage Range	3.15	3.45	V
1.8 Vcc Supply Voltage Range	1.7	1.9	V

20.3. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
Power Supply Current for Digital 3.3V	Icc	340	360	380	mA
Power Supply Current for Analog 3.3V	Icc	270	275	280	mA
Power Supply Current for Analog 1.8	Icc	160	230	300	mA

Parameter	SYM	Condition	Typical	Units
Power Supply Current for Digital 3.3V/Idle	Icc	No traffic on LAN/WAN/WLAN	340	mA
Power Supply Current for Digital 3.3V/TX/RX	Icc	Continue access LAN/WAN/WLAN	380	mA
Power Supply Current for Analog 3.3V/Idle	Icc	No traffic on LAN/WAN/WLAN	270	mA
Power Supply Current for Analog 3.3V/TX/RX	Icc	Continue access LAN/WAN/WLAN	280	mA
Power Supply Current for Analog 1.8/Idle	Icc	No traffic on LAN/WAN/WLAN	160	mA
Power Supply Current for Analog 1.8/TX/RX	Icc	Continue access LAN/WAN/WLAN	300	mA

20.4. AC Characteristics

20.4.1. Serial Interface Timing

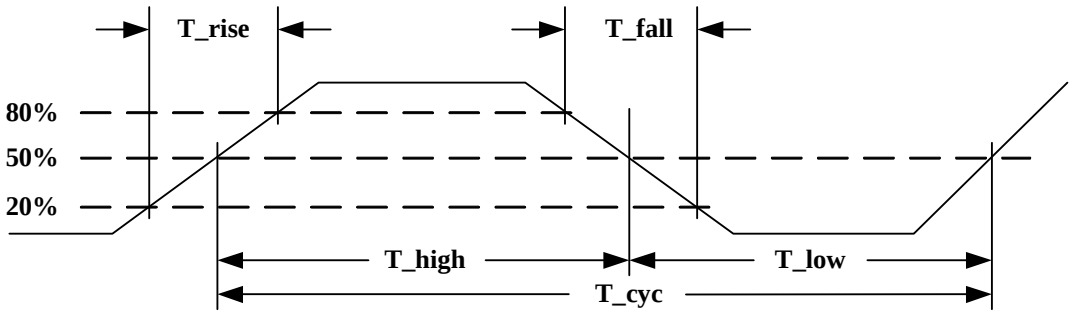


Figure 12. Clock Waveform

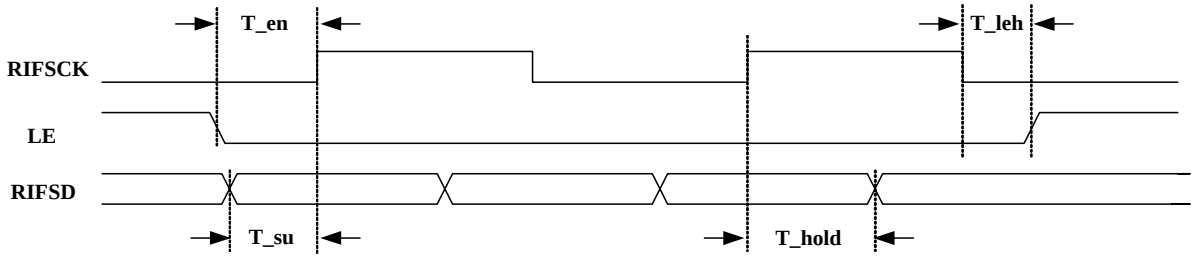


Figure 13. Serial Interface Timing

Table 100. Serial Interface Timing Parameters

Symbol	Parameter	Min	Max	Units
T_cyc	RIFSCK Cycle Time	40		ns
T_rise	RIFSCK Rise Time		40	ns
T_fall	RIFSCK Fall Time		40	ns
T_high	RIFSCK High Time	20		ns
T_low	RIFSCK Low Time	20		ns
T_su	RIFSD Setup Time	20		ns
T_hold	RIFSD Hold Time	10		ns
T_sv	LE to Status Valid	10		ns
T_leh	LE Hold Time	20		ns

Table 101. Intersil Chipset Serial Data Format

First Bit											Last Bit
B20	B19	B18	B17	B16	B15 ~ B7	B6	B5	B4	B3	B2	B1
Data Field										Register Definition	

Table 102. RFMD Chipset Serial Data Format

First Bit															Last Bit
D17	D16	D15	D14	D13..D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
Data Field												Address Field			

Table 103. Philips Chipset Serial Data Format

First Bit															
A0	A1	A2	A3	A4	A5	A6	RW	D0	D1	D2	D3	D4	D5	D6	D7
Address Field							RW	Data Field							

														Last Bit	
D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23
Data Field															

Note: For programming serial control registers, please refer to the Intersil, RFMD, or Philips' datasheets.

20.5. RF Control Timing

Table 104. RF Control Timing

Symbol	Parameter	Delay	Tolerance	Units
T_d1	PE2 to TRSW	2	±0.1	µs
T_d2	PE2 to PAPE	3	±0.1	µs
T_d3	PAPE to TXIQ	Controlled by PAPE_sign (bit 2, Config 2) and PAPE_time (bits 1:0, Config 2)	±0.1	µs
T_d4	PAPE to PE2	3	±0.1	µs
T_d5	TRSW to PE2	2	±0.1	µs

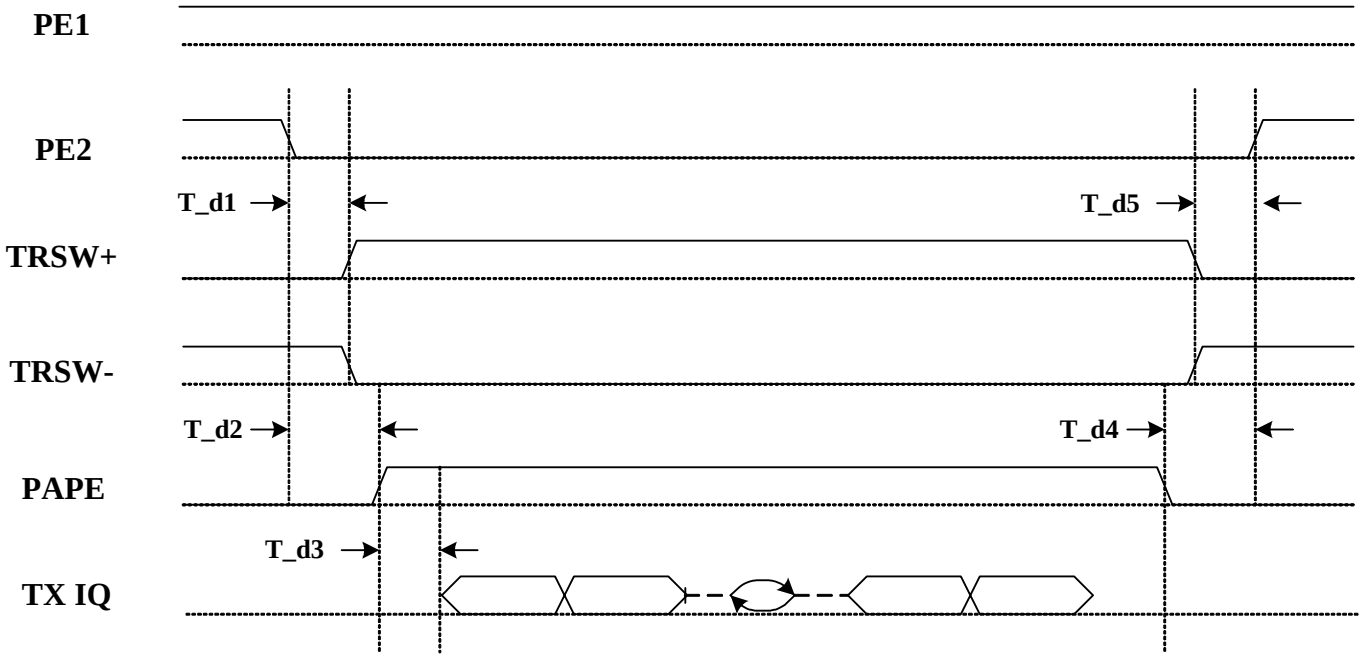


Figure 14. Intersil Chipset Transmit Control Signal Sequencing

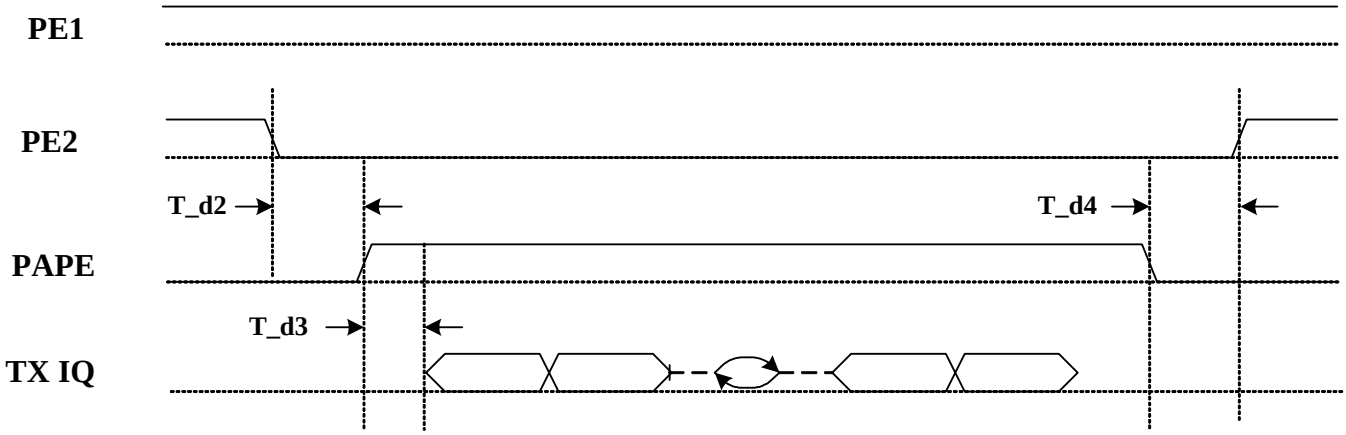


Figure 15. RFMD Chipset Transmit Control Signal Sequencing

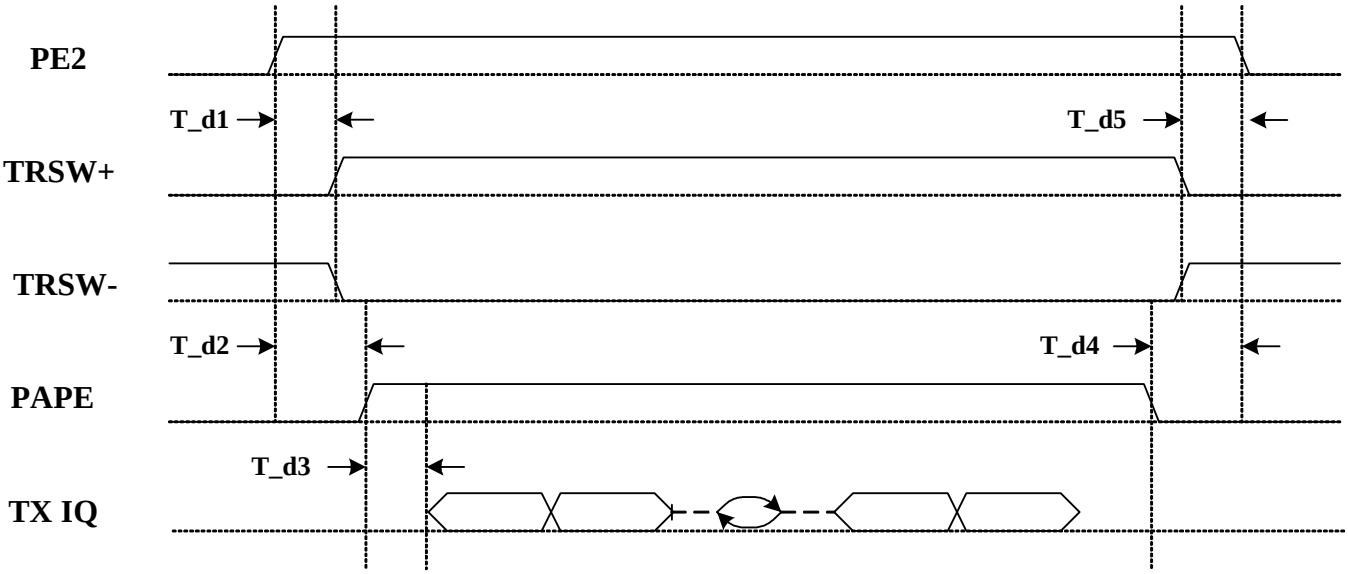


Figure 16. Philips Chipset Transmit Control Signal Sequencing

20.6. Digital Timing Characteristics

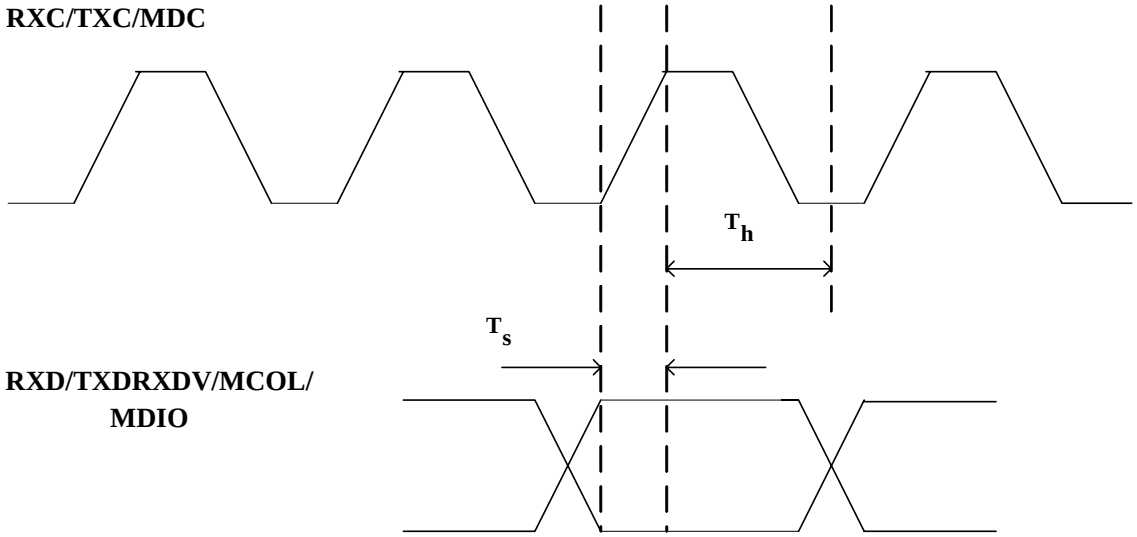


Figure 17. Digital Timing Characteristics

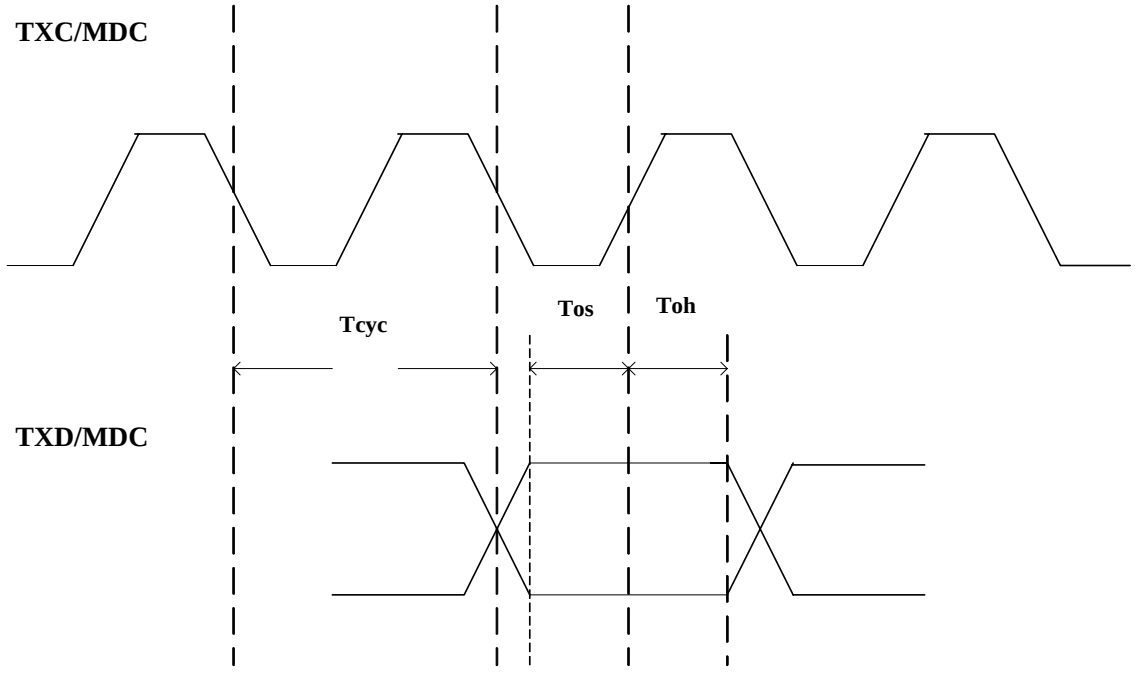


Figure 18. MII DC Timing

Table 105. Digital Timing Characteristics

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
100M TXC/RXC	T_{cyc}	TXC/RXC clock cycle time.	I		40±50ppm		ns
10M TXC/RXC	T_{cyc}	TXC/RXC clock cycle time.	I		400±500ppm		ns
TXD/RXD/TXEN/RXDV Output Setup time	T_{os}	Output Setup time from TXC/RXC rising edge to TXD/RXD/TXEN/RXDV.	O	22	24	26	ns
TXD/RXD/TXEN/RXDV Output Hold time	T_{oh}	Output Setup time from TXC/RXC rising edge to TXD/RXD/TXEN/RXDV.	O	14	16	18	ns
RXD/RXDV/COL Setup time	T_s	RXD/RXDV/TXEN/COL to RXC/TXC rising edge setup time.	I	4			ns
RXD/RXDV/COL Setup time	T_h	RXD/RXDV/TXEN/COL to RXC/TXC rising edge hold time.	I	2			ns

21. Design and Layout Guide

In order to achieve maximum performance using the RTL8181/RTL8181P, good design attention is required throughout the design and layout process. The following are some recommendations on how to implement a high performance system.

General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV).
- Keep power and ground noise levels below 50mV.
- Use bulk capacitors (4.7µF-10µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8181/RTL8181P chip.

Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonally or separate by a ground plane.

Clock Circuit

- If possible, surround the clock by ground trace to minimize high-frequency emissions.
- Keep the crystal or oscillator as close to the RTL8181/RTL8181P as possible.

Power Plane

- Divide the power plane into 1.8V digital, 3.3V analog, and 3.3V digital.
- Use 0.1µF decoupling capacitors and bulk capacitors between each power plane and the ground plane.

Ground Plane

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.

RF Interface

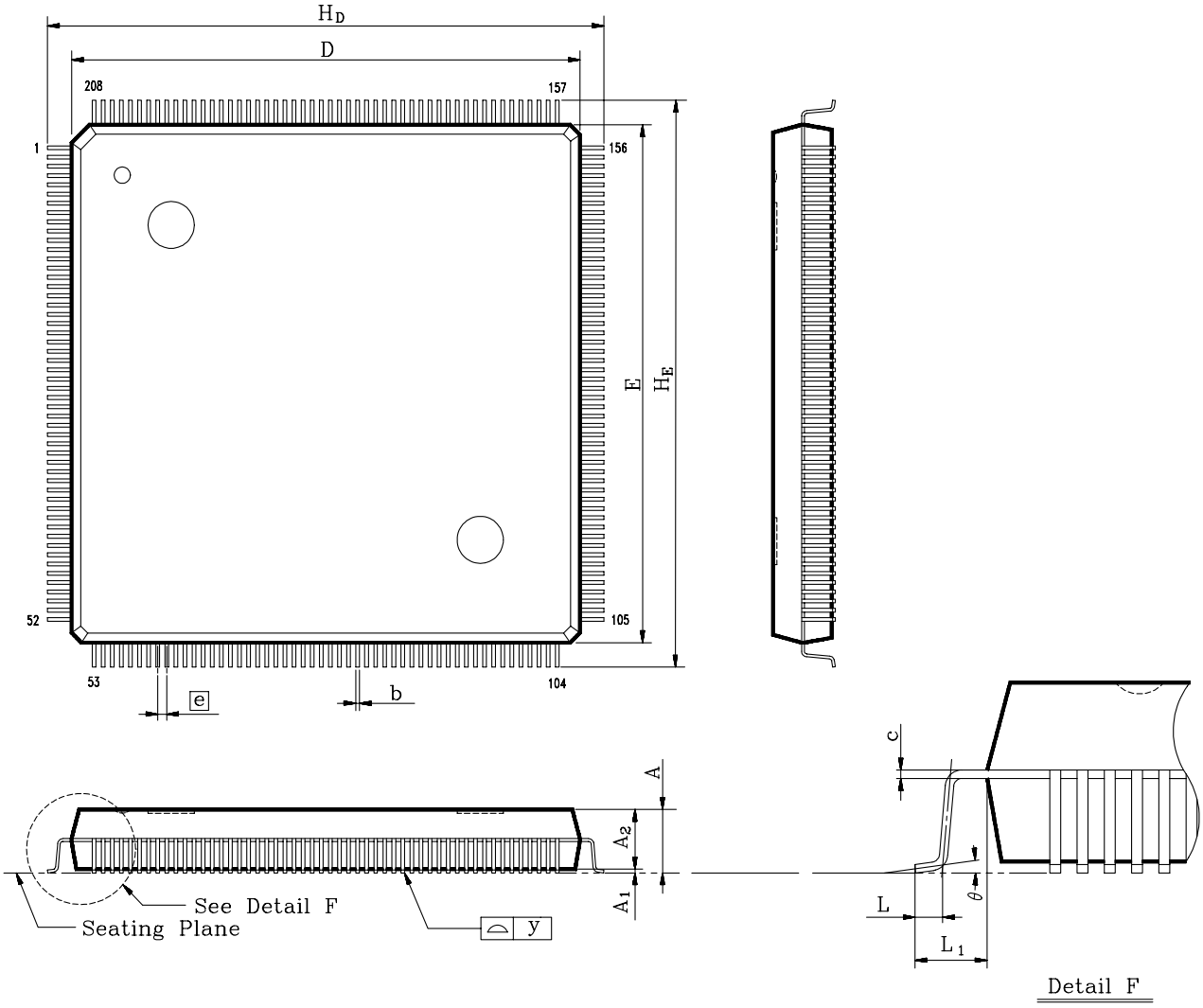
- As the RF interface is complex and power noise sensitive, we strongly recommend customers to hard copy the RF design from Realtek.

Memory Interface

- Keep the SDRAM as close as possible to the RTL8181/RTL8181P. The FLASH timing is slower than SDRAM so place the SDRAM closer than FLASH if space considerations prevent placing both components equally close to the RTL8181/RTL8181P.
- Where two banks of SDRAM are used, the memory clock trace should have the same length.

22. Mechanical Dimensions

22.1. Package Outline for 208 LQFP (28*28*1.4mm)



See the Mechanical Dimensions notes on the next page.

22.2. Notes for 208 LQFP

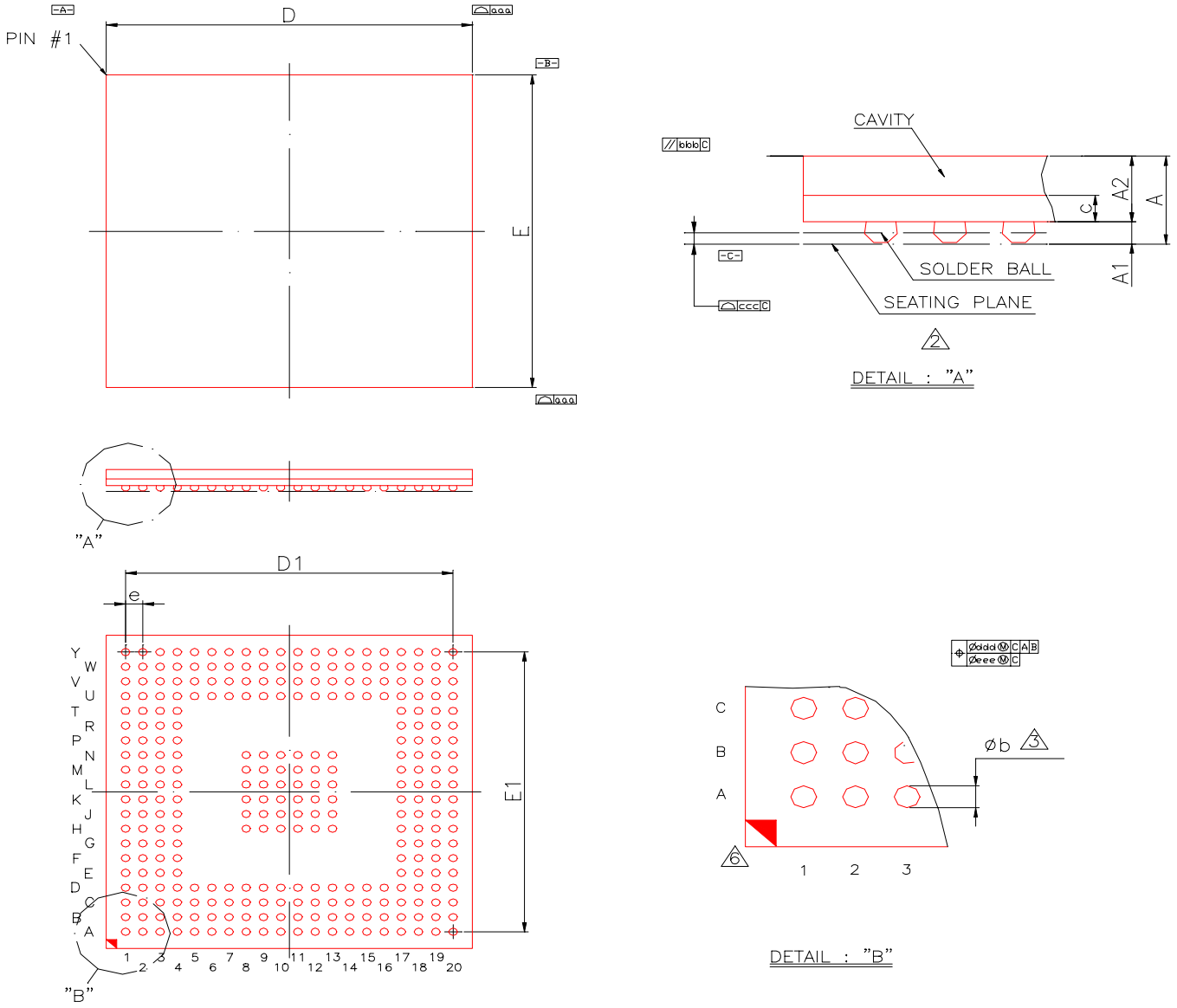
Symbol	Dimension in inch			Dimension in mm		
	Min	Typ	Max	Min	Typ	Max
A	0.136	0.144	0.152	3.45	**3.65**	3.85
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.119	0.128	0.136	3.02	**3.24**	3.46
b	0.004	0.008	0.012	0.10	**0.20**	0.30
c	0.002	0.006	0.010	0.04	**0.15**	0.26
D	1.093	1.102	1.112	27.75	**28.00**	28.25
E	1.093	1.102	1.112	27.75	**28.00**	28.25
e	0.012	0.020	0.031	0.30	**0.50**	0.80
HD	1.169	1.205	1.240	29.70	**30.60**	31.50
HE	1.169	1.205	1.240	29.70	**30.60**	31.50
L	0.010	0.020	0.030	0.25	**0.50**	0.75
L1	0.041	0.051	0.061	1.05	**1.30**	1.55
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : 208L QFP (28x28 mm*2) FOOTPRINT 2.6mm PACKAGE OUTLINE DRAWING			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	
		PAGE	
CHECK		DWG NO.	
		DATE	
REALTEK SEMICONDUCTOR CORP.			

22.3. Package Outline for TFBGA 292 BALL (17*17 mm)



See the Mechanical Dimensions notes on the next page.

22.4. Notes for TFBGA 292 BALL

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.30	---	---	0.051
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	013	0.014	0.016
D	16.90	17.00	17.10	0.665	0.669	0.673
E	16.90	17.00	17.10	0.665	0.669	0.673
D1	---	15.20	---	---	0.598	---
E1	---	15.20	---	---	0.598	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.12			0.005		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	20/20			20/20		

Notes:

1. CONTROLLING DIMENSION: MILLIMETER
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT: JEDEC MO-205.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

TITLE : 292LD TFBGA (17x17mm) PACKAGE OUTLINE			
SUBSTRATE MATERIAL: BT RESIN			
APPR.		DWG NO.	
ENG.		Rev NO	
QM.		PRODUCT CODE	
CHK.		DATE.	
DWG.		SHT No.	
REALTEK SEMICONDUCTOR CORP.			

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