

SLIC-DC
- 2 RJ-11 connectors
(for FXS)

CPC5621
- 1 RJ-11 connectors
(for FXO)

UART_USB
- 1 UART driver
DB-9 connector x 1
- 2 USB type-A
connector

RJ-45
- 5 RJ-45 connectors
(for 10/100 PHY)

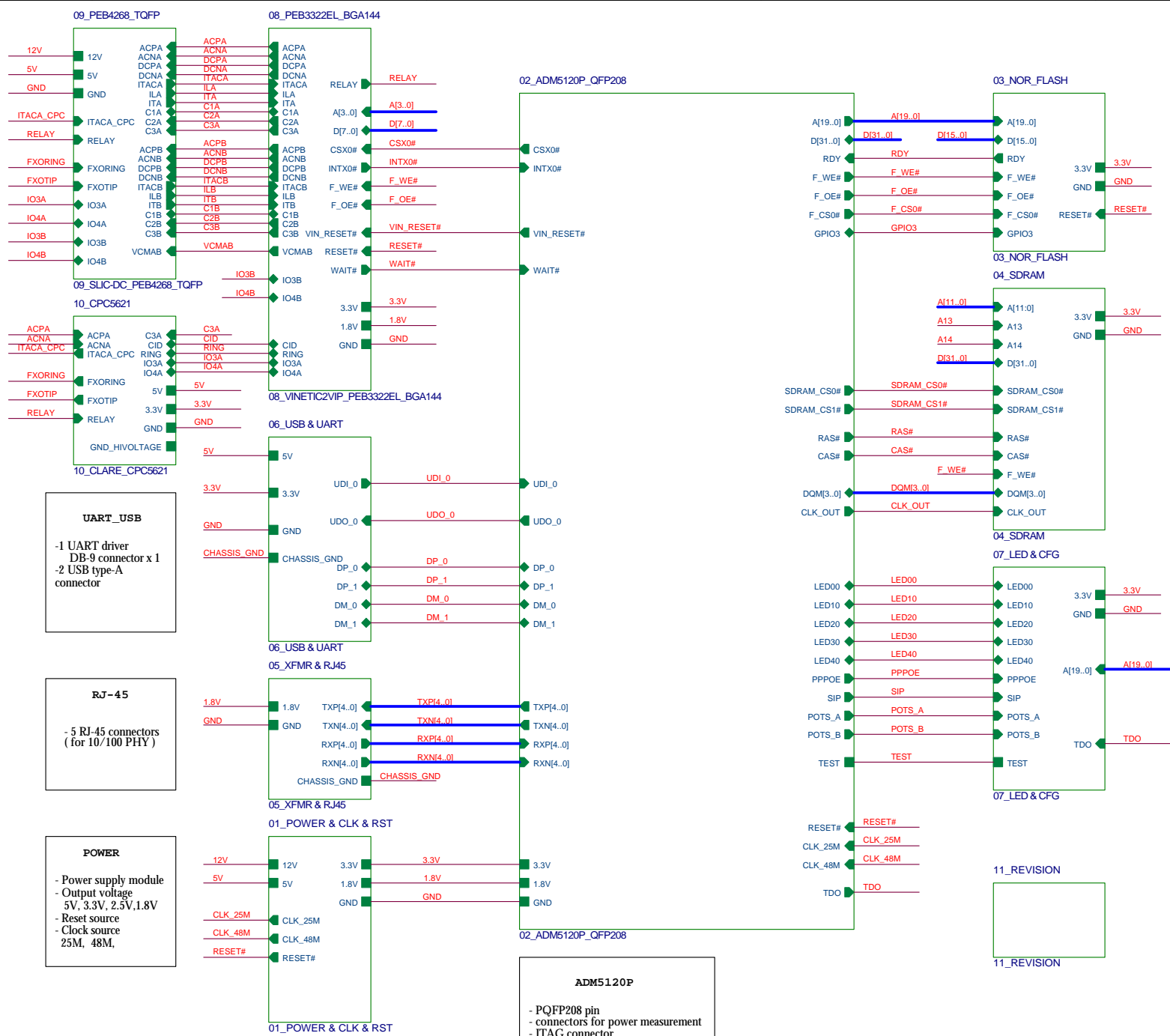
POWER
- Power supply module
- Output voltage
5V, 3.3V, 2.5V, 1.8V
- Reset source
25M, 48M,

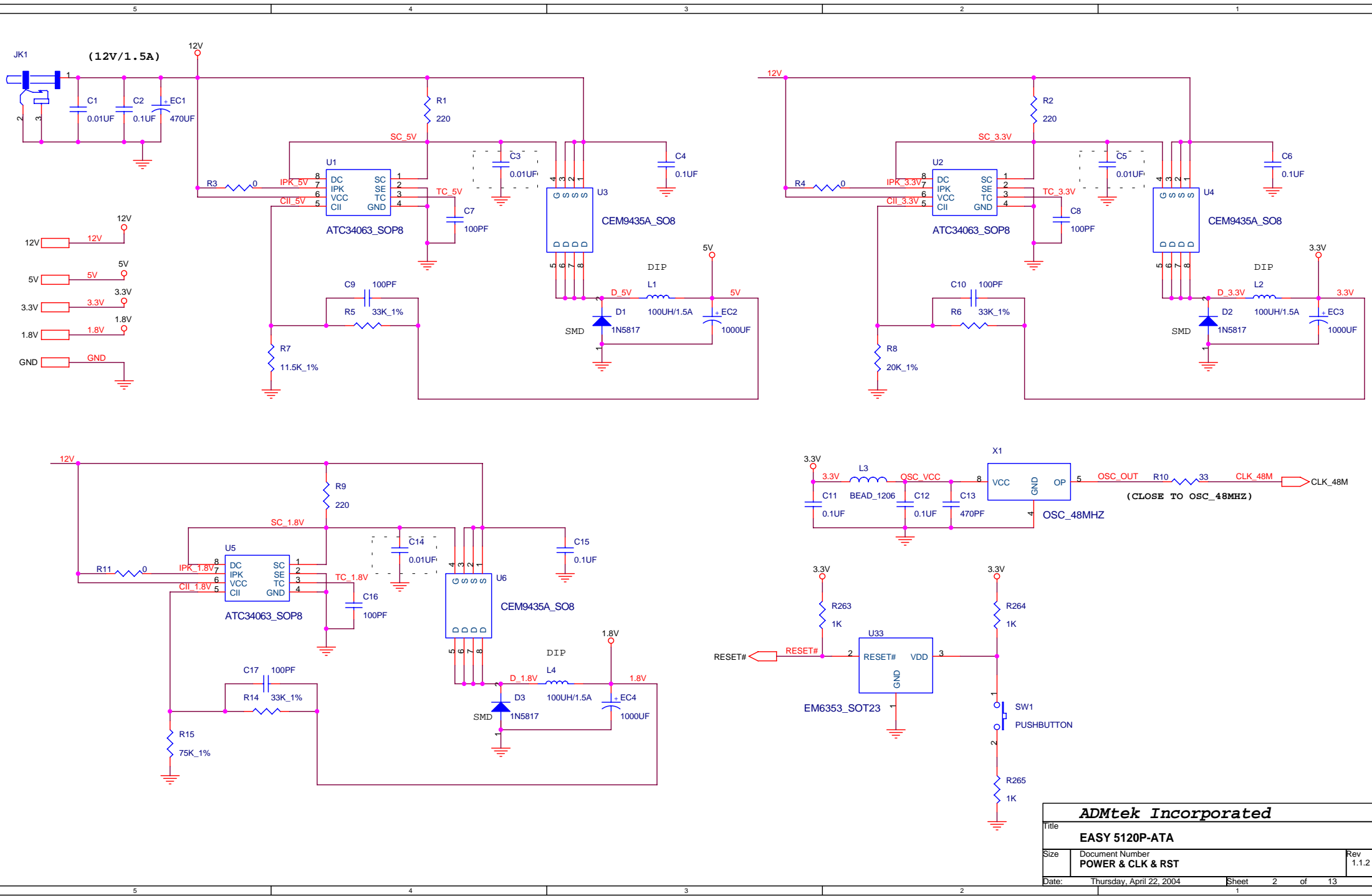
ADM5120P
- PQFP208 pin
- connectors for power measurement
- JTAG connector

NOR_FLASH
- NOR type flash
2M x 16 or 1M x 16

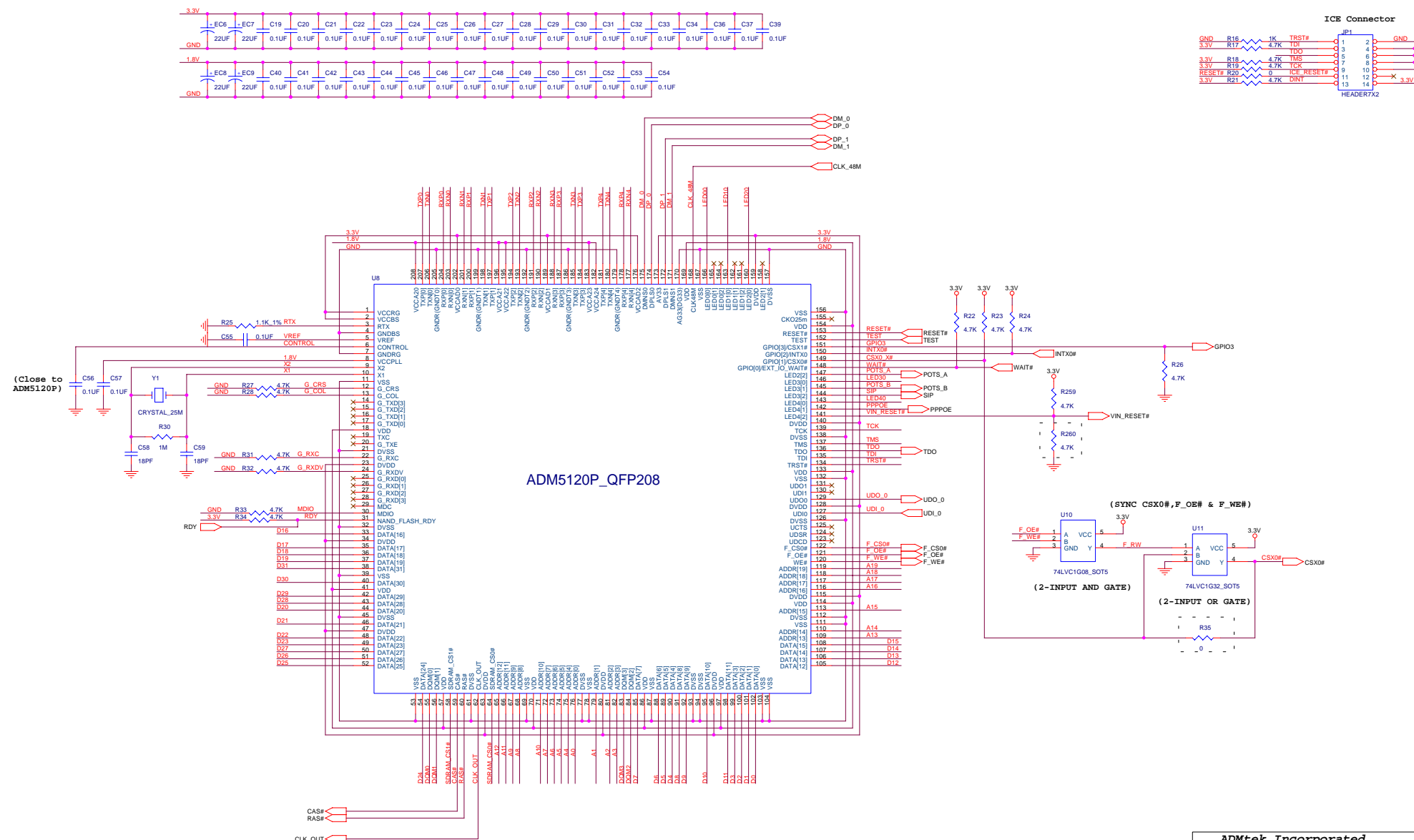
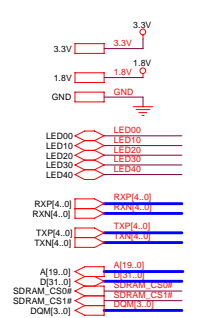
SDRAM
- 2M x 32 x 2 Banks winbond's SDRAM

LED & CFG
- Pin Strapping
- Power LED
- LED for 5 10/100 ports
- LED for 2 POTS port
- PPPoE LED
- SIP LED



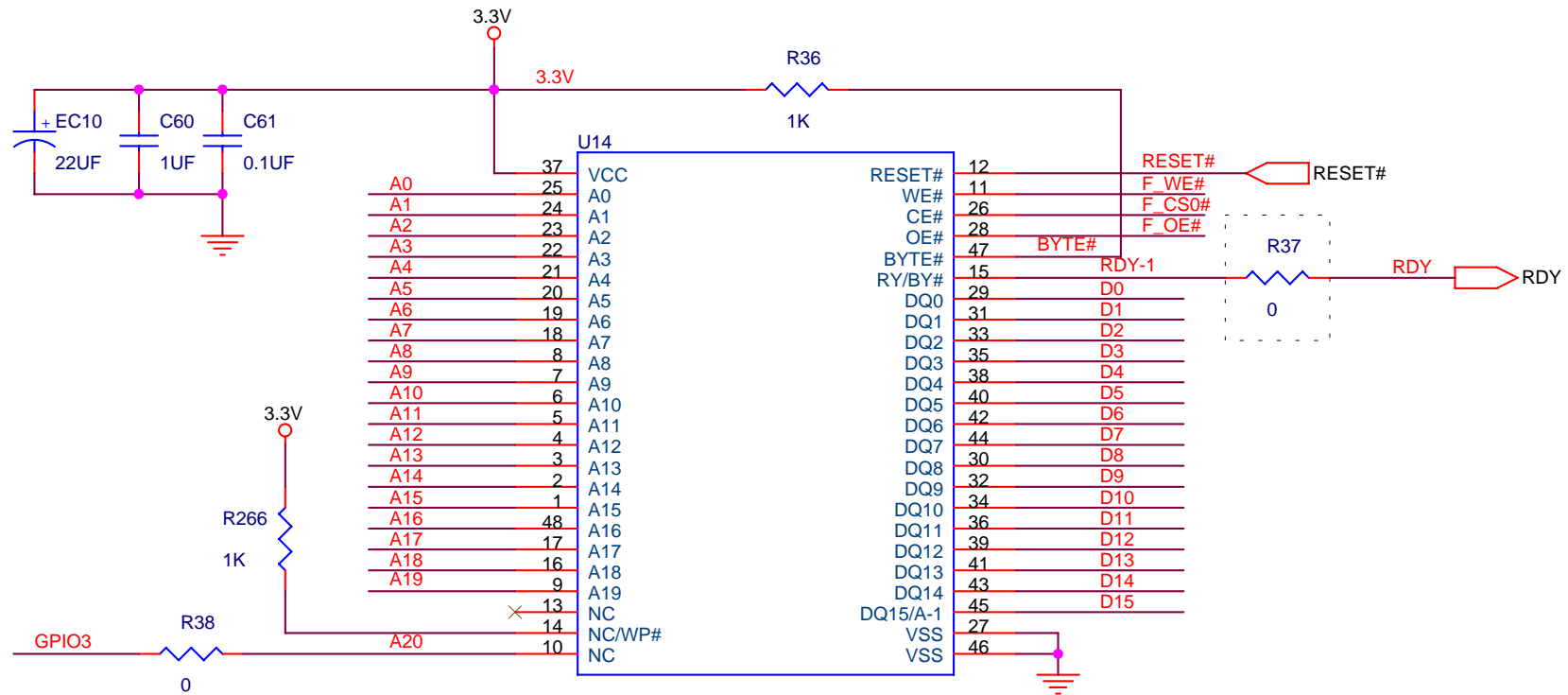
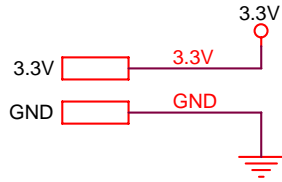
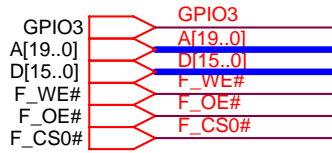


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Title EASY 5120P-ATA		
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ADM5120P_QFP208

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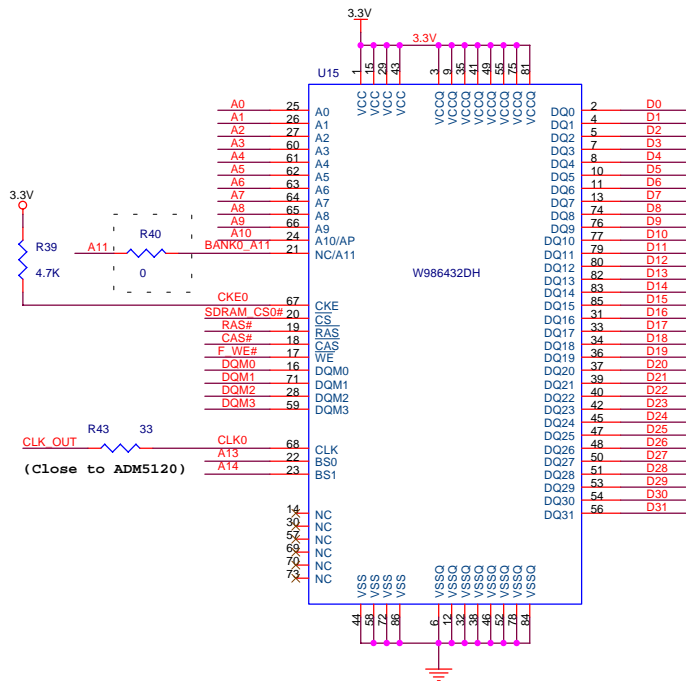
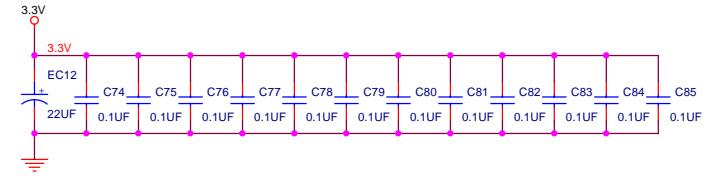
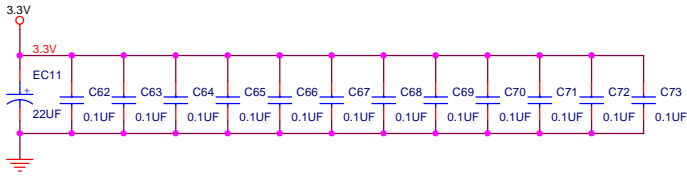
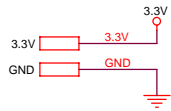
(For MX29LV320(2Mx16))

MX29LV320(2Mx16)
 (Or MX29LV160(1Mx16))

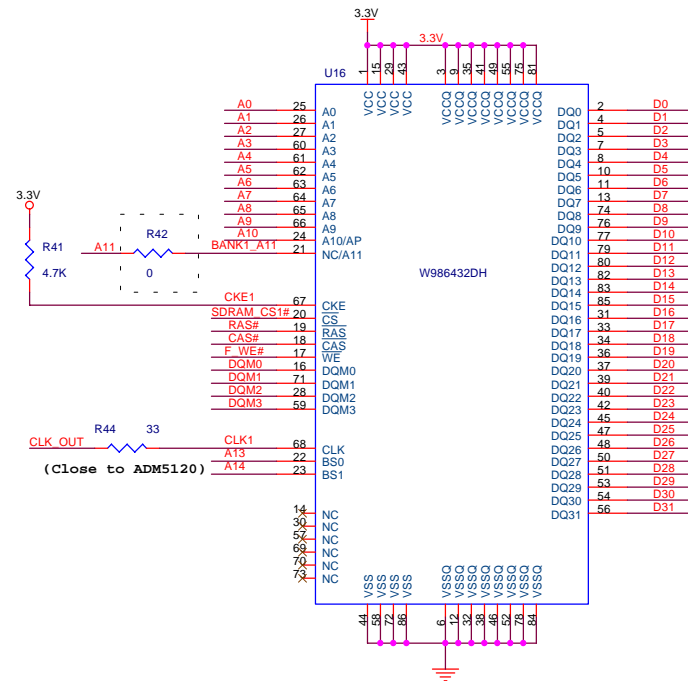
ADMtek Incorporated

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EASY 5120P-ATA		
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	NOR_FLASH	1.1.2

A[11..0] → A11..01
 A13 → A13
 A14 → A14
 DQM[3..0] → DQM3..01
 CAS# → CAS#
 RAS# → RAS#
 SDRAM_CS0# → SDRAM_CS0#
 SDRAM_CS1# → SDRAM_CS1#
 D[31..0] → D31..01
 CLK_OUT → CLK_OUT
 F_WE# → F_WE#

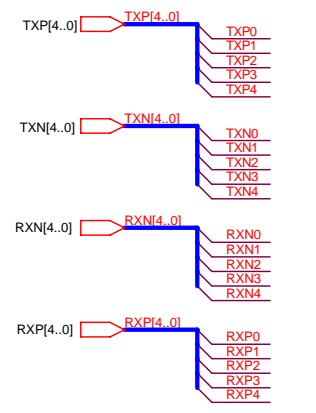
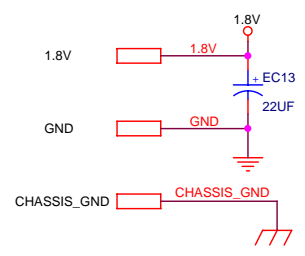


W986432DH (2Mx32)
SDRAM Bank 0

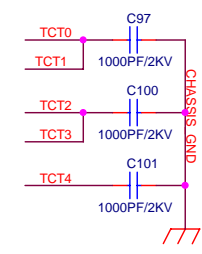
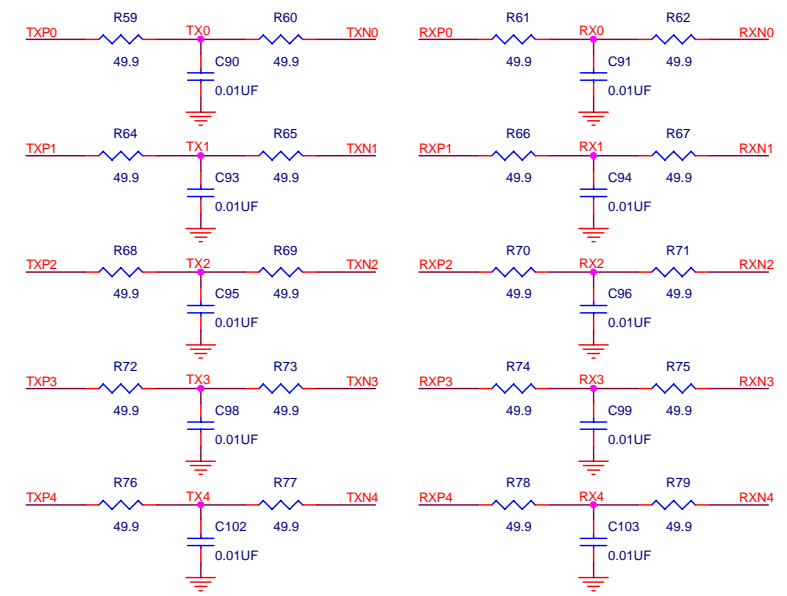
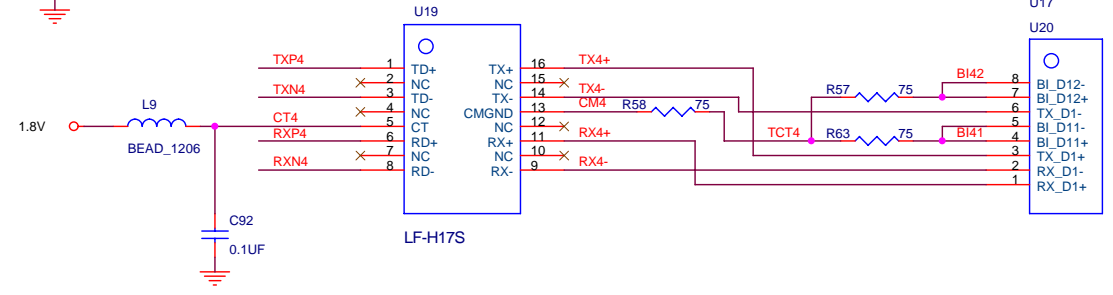
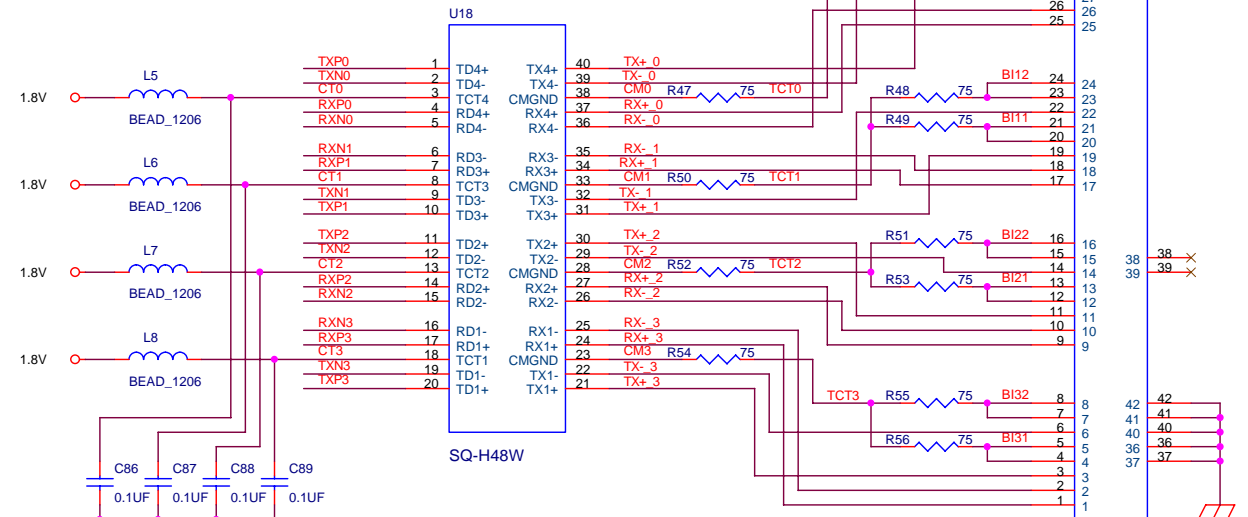


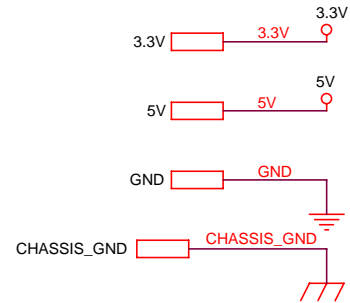
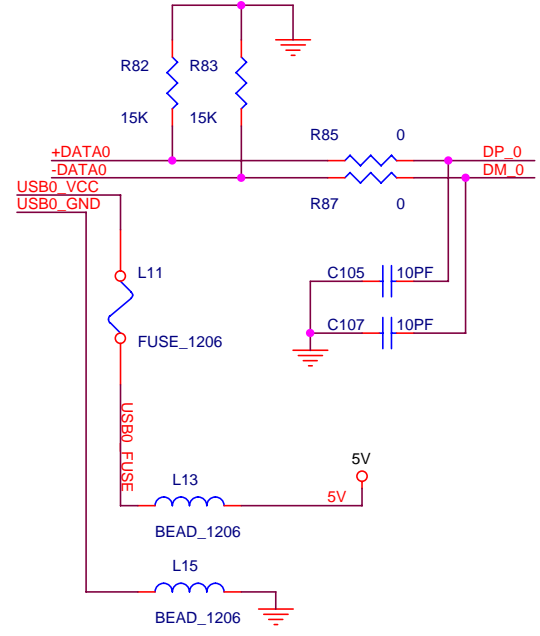
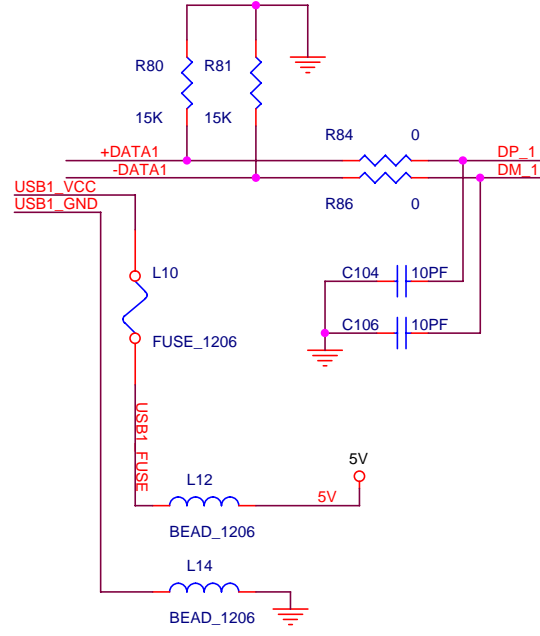
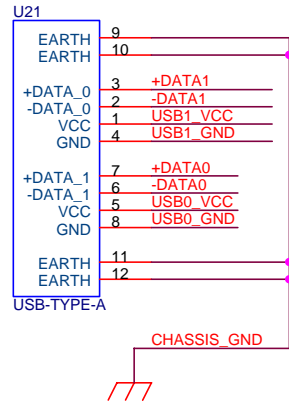
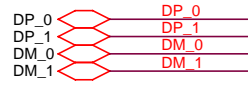
W986432DH (2Mx32)
SDRAM Bank 1

ADMTek Incorporated		
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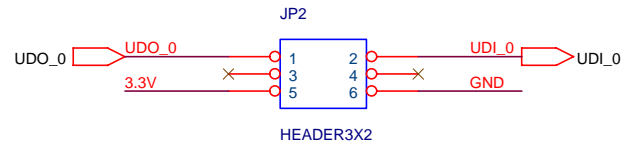


AUTO MDIX

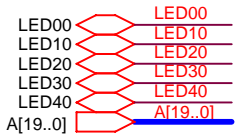
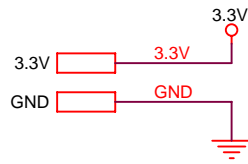




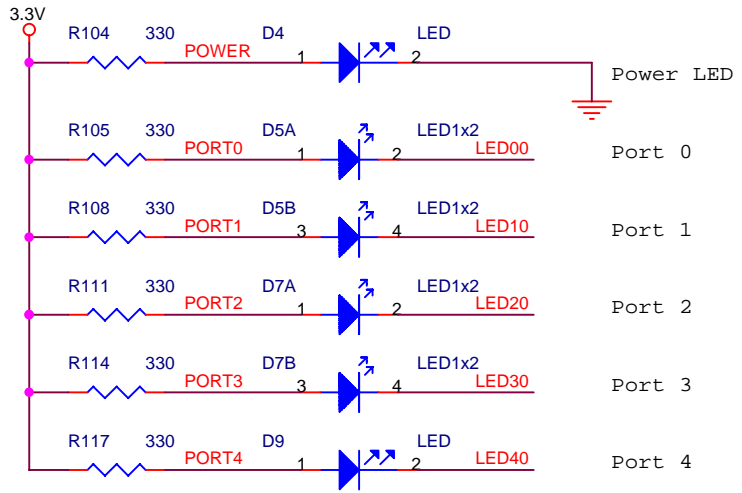
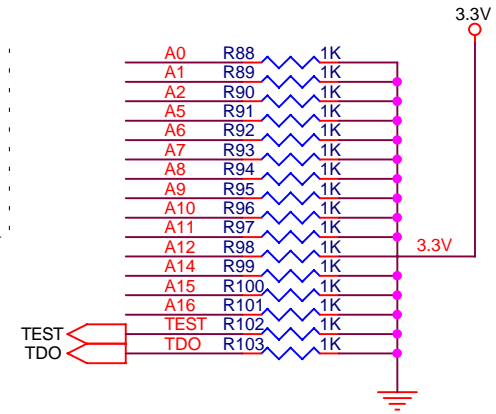
UART Connector



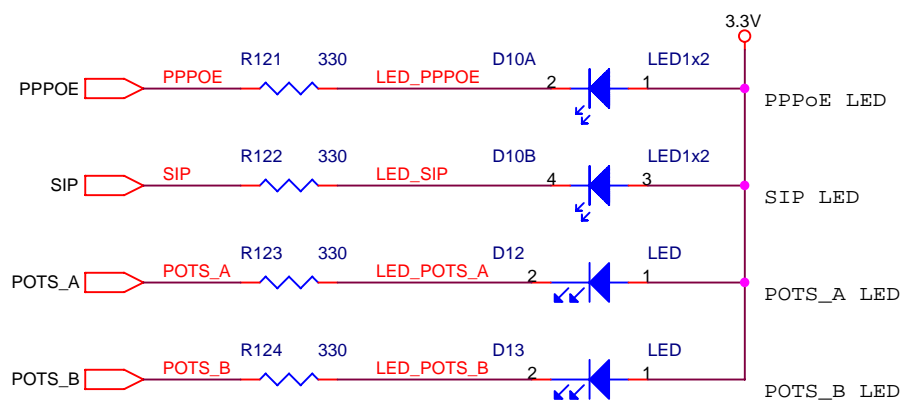
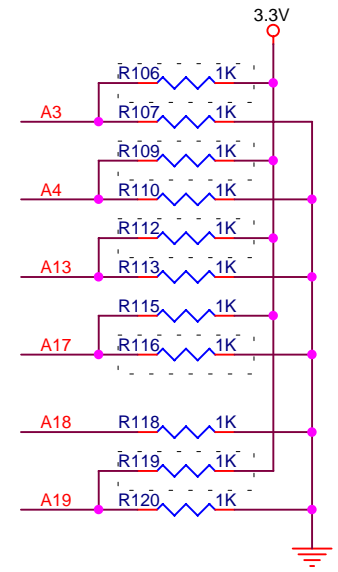
ADMtek Incorporated		
EASY 5120P-ATA		
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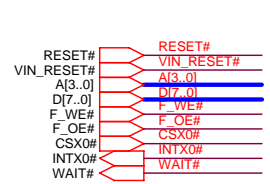


A1: NAND boot, pull down to disable
 A2: Auto MDIX, pull down to enable
 A12: Model, pull up to QFP package
 (for internal use)
 TEST, TDO: TEST mode,
 pull down for normal use.

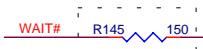
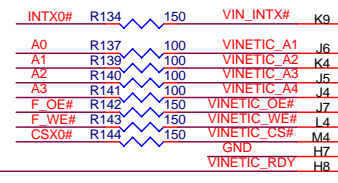
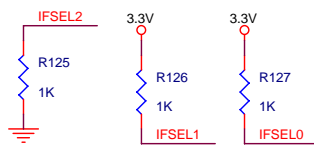


A4-A3: Pll setting
 00=175MHz (default)
 01=200MHz
 10,11=Reserved
 A13: Separate Power,
 0: PHY separate power on disable
 (default)
 1: PHY separate power on enable
 A18-A17: Nor flash boot
 00: boot in 8 bit.
 01: boot in 16 bit. (default)
 10,11: Reserved
 A19: endian
 0: little endian (default)
 1: big endian

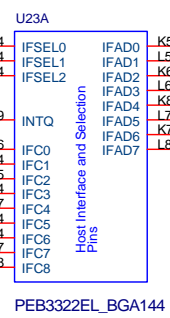
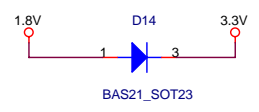
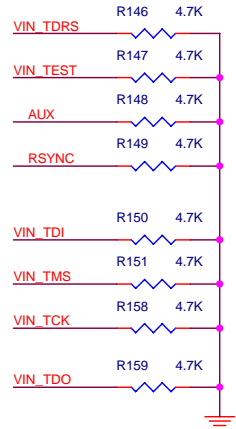
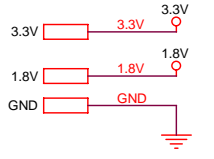




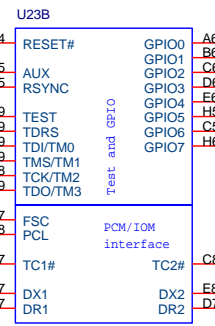
IFSEL[2:0]:Interface-Type Selection
(011:8-bit INTEL demultiplexed mode)



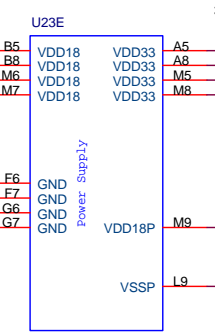
(For VINETIC2)



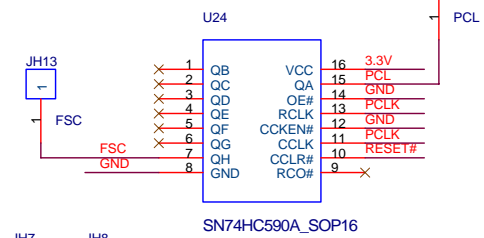
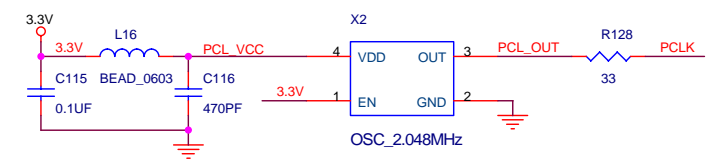
PEB3322EL_BGA144



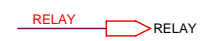
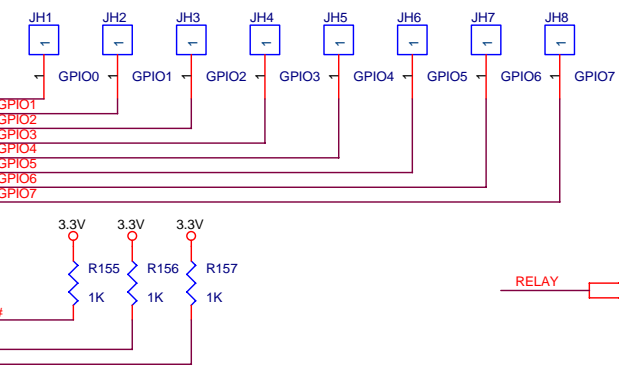
PEB3322EL_BGA144



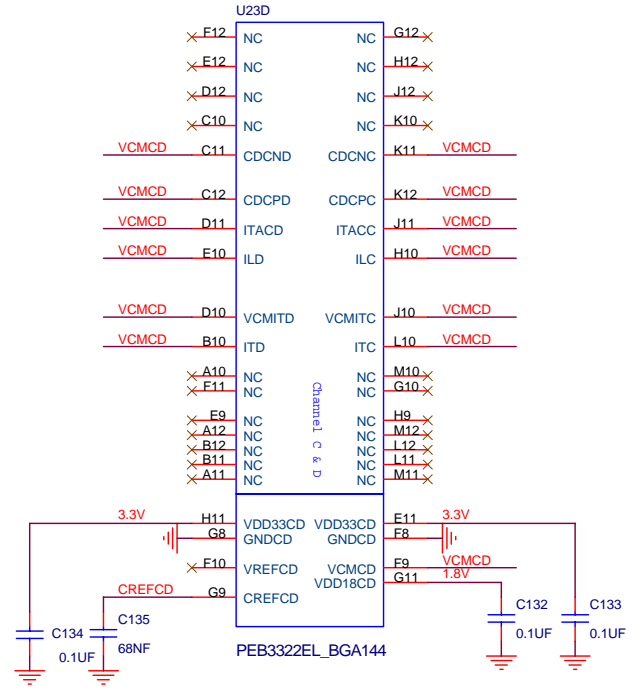
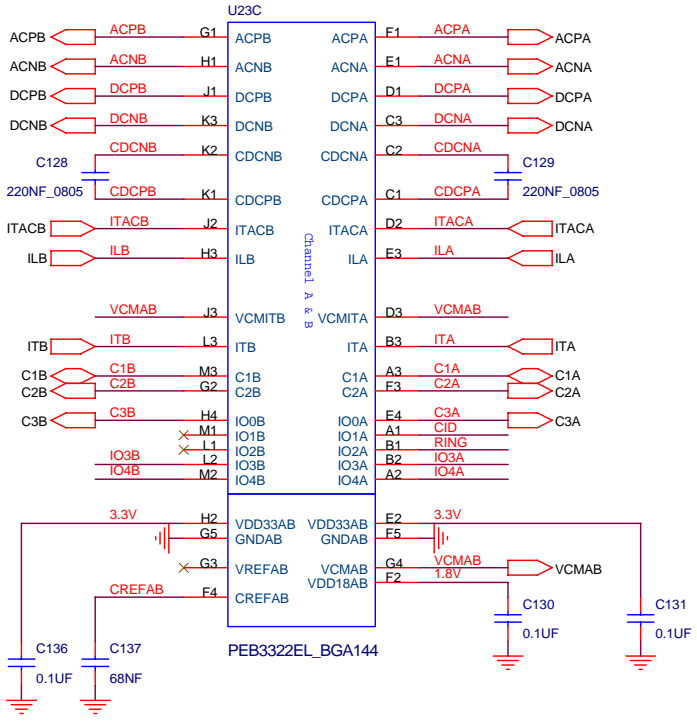
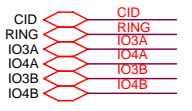
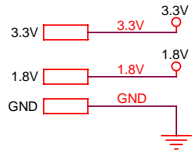
PEB3322EL_BGA144



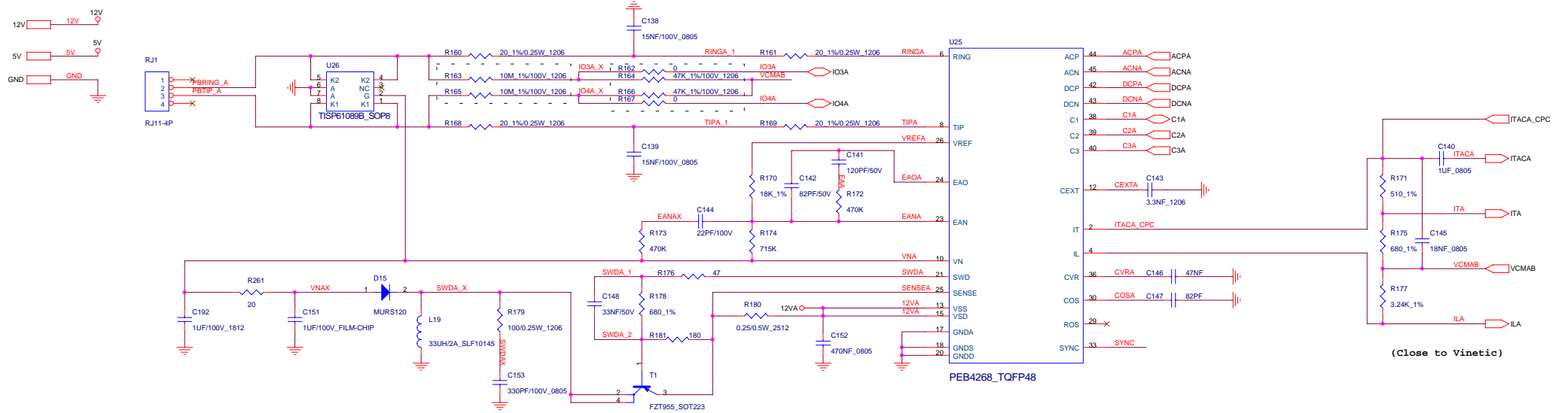
(8-BIT COUNTER WITH 3-OUTPUT REGISTER)
(PCL:1.024MHz)
(FSC:8KHz)



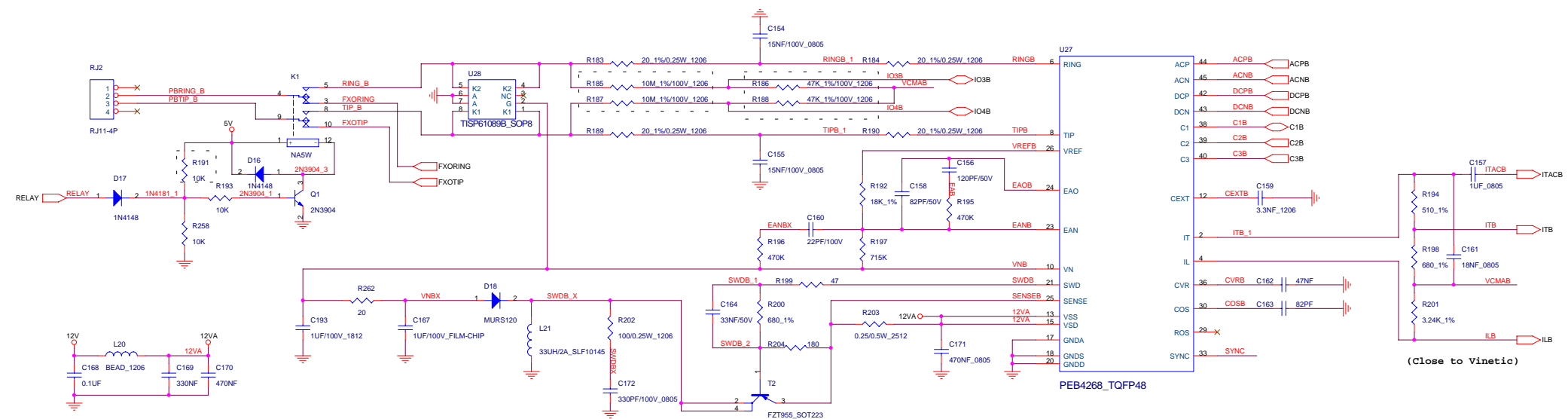
ADMtek Incorporated		
EASY 5120P-ATA		
Size	Document Number	Rev
	VINETIC-2VIP_PEB3322EL_BGA144_DIGITAL_PART	1.1.2
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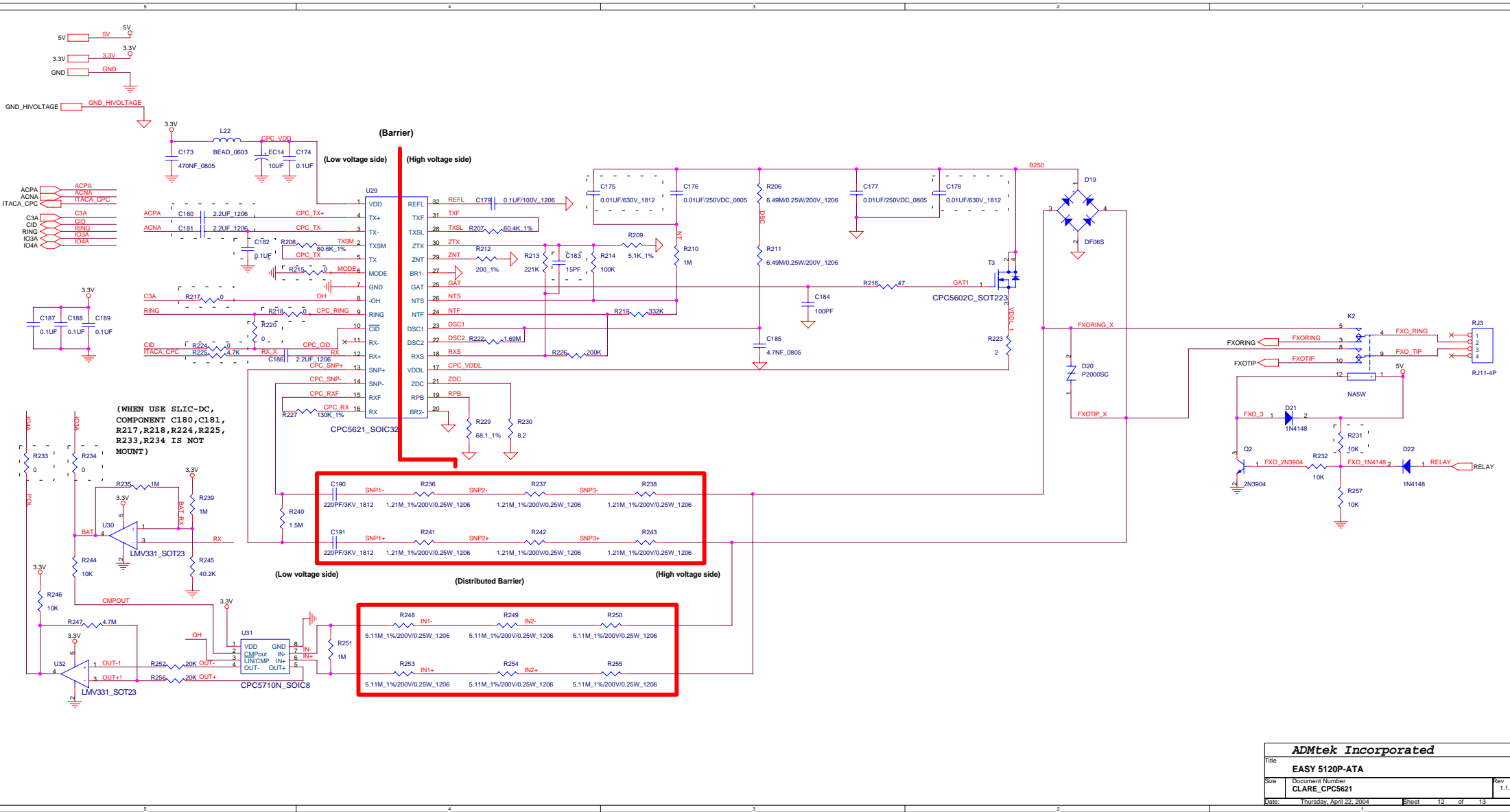
ADMtek Incorporated		
Title EASY 5120P-ATA		
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(Close to Vinetic)



(Close to Vinetic)



Rev	Modification
1.0	- First draft
1.1	- SLIC-DC major change release state
1.1.1	<ul style="list-style-type: none"> - Change EC2 , EC3 , EC4 from 220uF to 1000uF - Add pull up resistor R266 for MX29LV320 WP# pin (this resistor doesn't exist in V1.1 PCB) - Change D15 , D18 pin define
1.1.2	<ul style="list-style-type: none"> - Change C7 , C8 , C16 from 470pF to 100pF - change R3 , R4 , R11 from 0.22 to 0 - change R1 , R2 , R9 from 100 to 220

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EASY 5120P-ATA		
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	REVISION	1.1.2
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