

SLIC-DC
- 2 RJ-11 connectors
(for FXS)

CPC5621
- 1 RJ-11 connectors
(for FXO)

UART_USB
- 1 UART driver
DB-9 connector x 1
- 2 USB type-A
connector

RJ-45
- 5 RJ-45 connectors
(for 10/100 PHY)

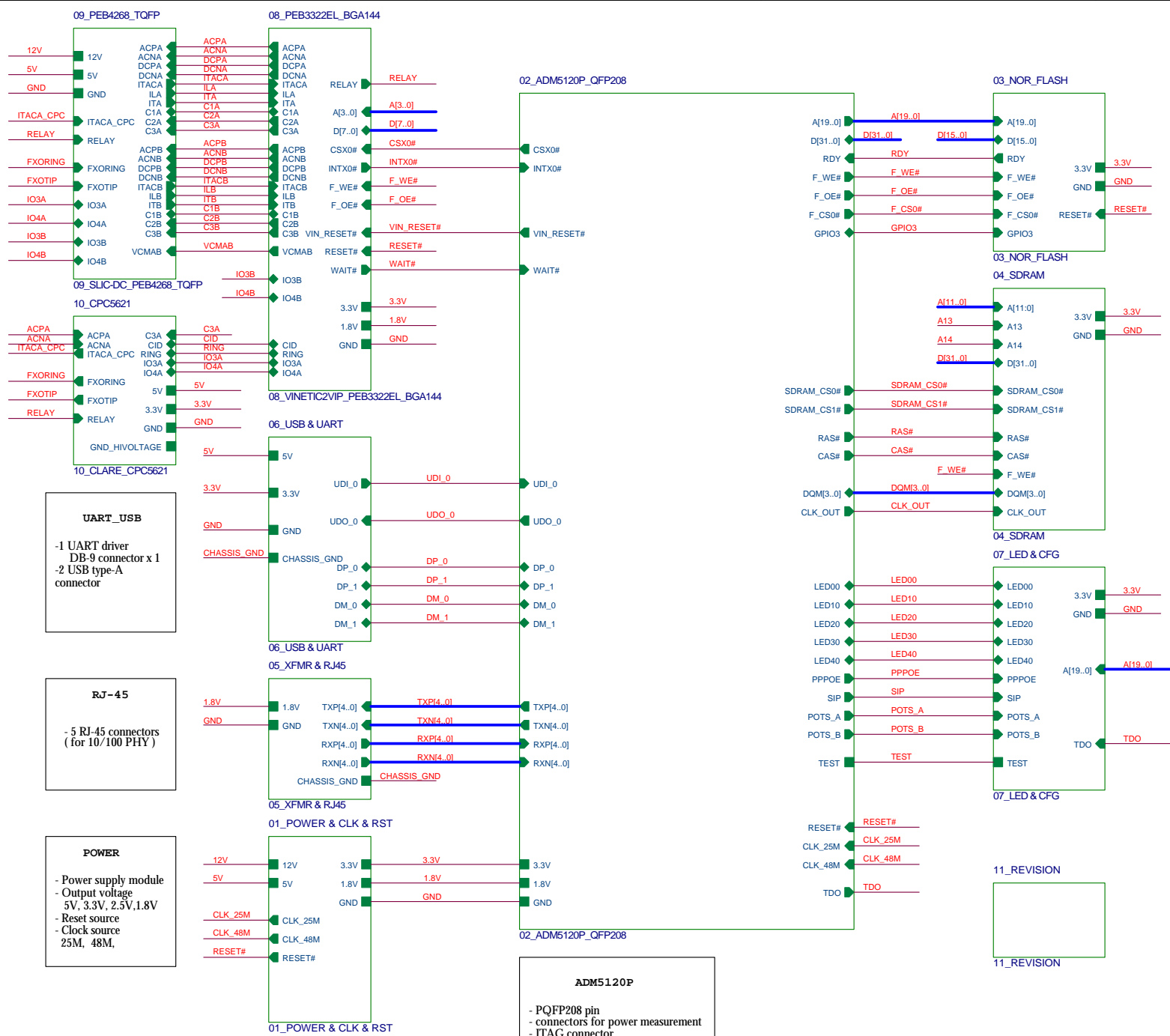
POWER
- Power supply module
- Output voltage
5V, 3.3V, 2.5V, 1.8V
- Reset source
- Clock source
25M, 48M,

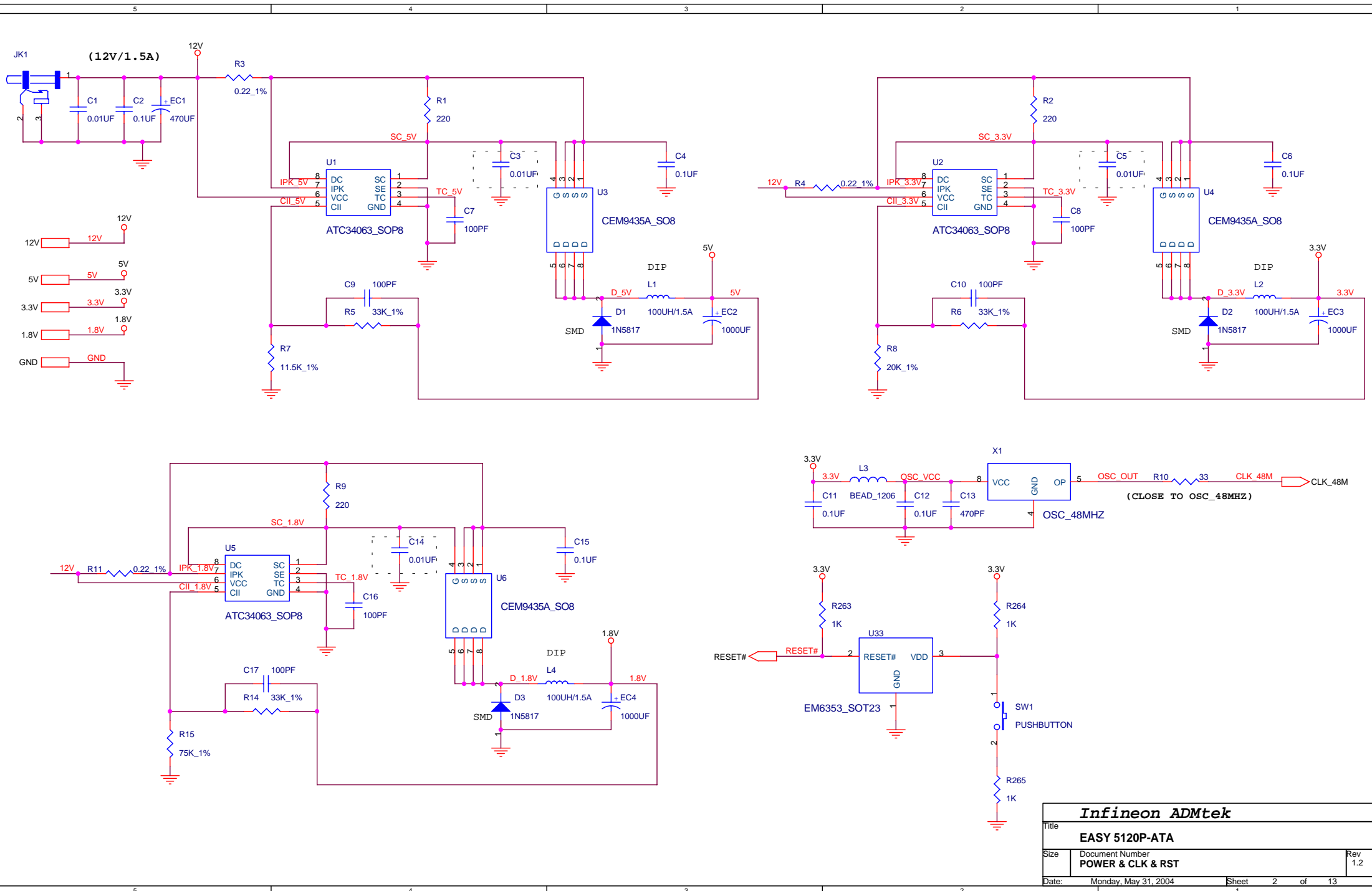
ADM5120P
- PQFP208 pin
- connectors for power measurement
- JTAG connector

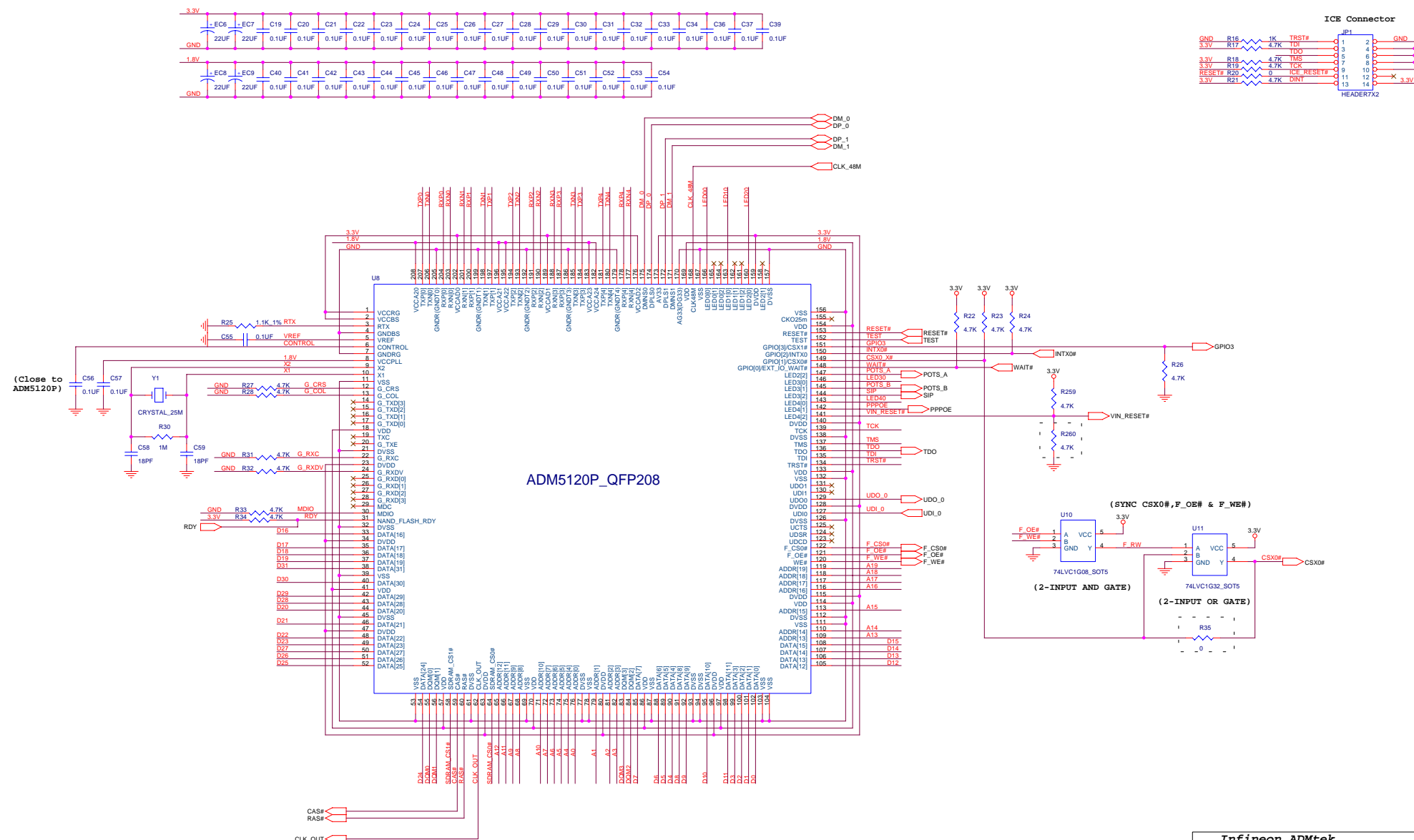
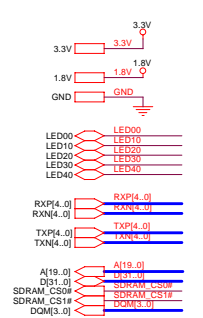
NOR_FLASH
- NOR type flash
2M x 16 or 1M x 16

SDRAM
- 2M x 32 x 2 Banks winbond's SDRAM

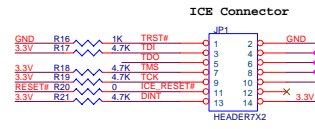
LED & CFG
- Pin Strapping
- Power LED
- LED for 5 10/100 ports
- LED for 2 POTS port
- PPPoE LED
- SIP LED



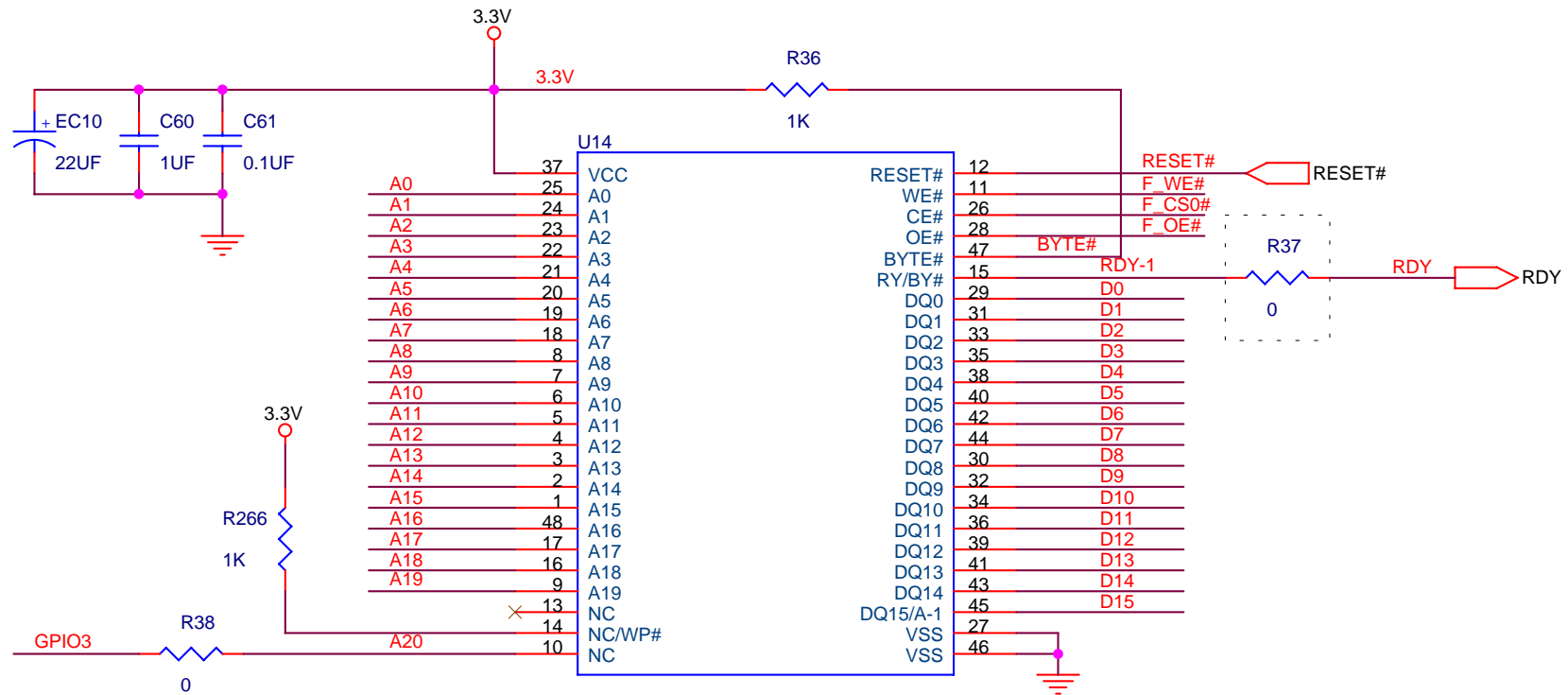
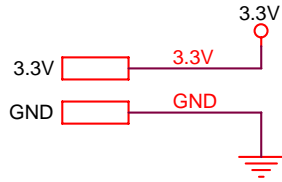
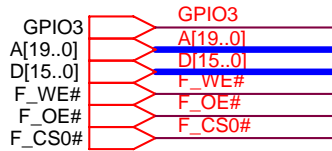




ADM5120P_QFP208



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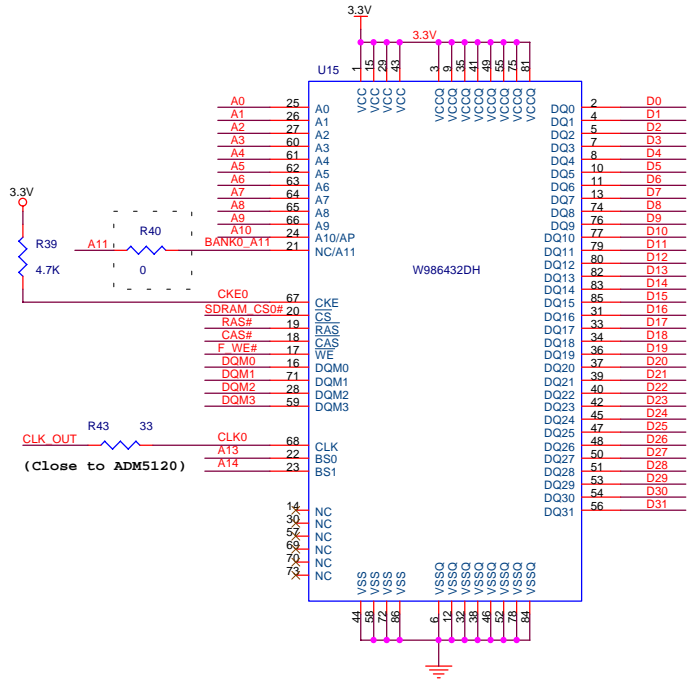
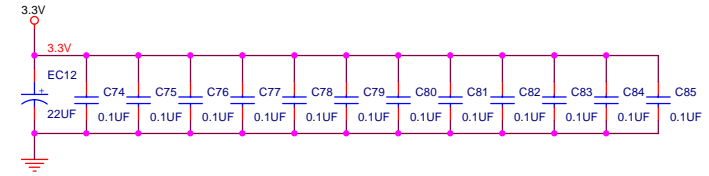
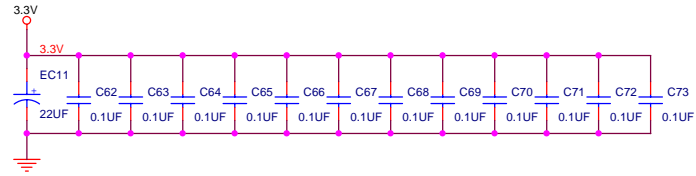
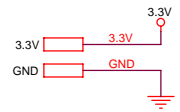
(For MX29LV320(2Mx16))

MX29LV320 (2Mx16)
(Or MX29LV160 (1Mx16))

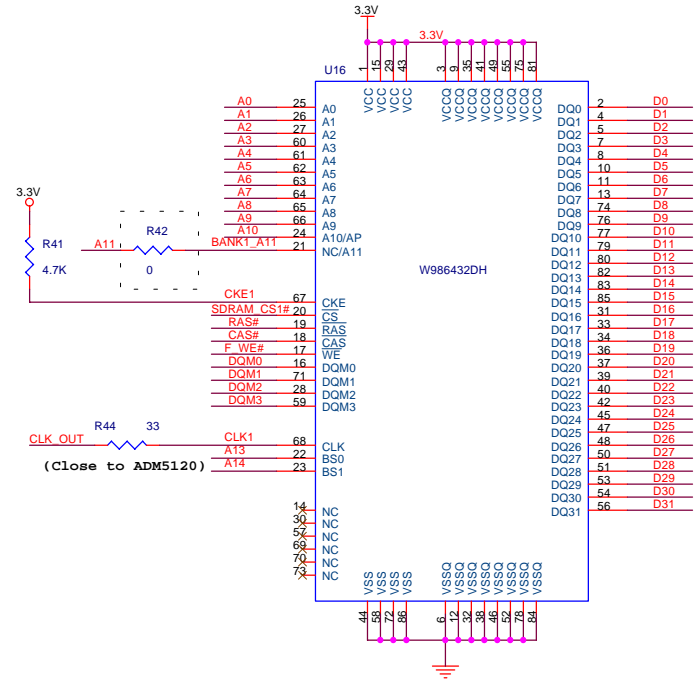
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- A[11..0] → A11..01
- A13 → A13
- A14 → A14
- DQM[3..0] → DQM3..01
- CAS# → CAS#
- RAS# → RAS#
- SDRAM_CS0# → SDRAM_CS0#
- SDRAM_CS1# → SDRAM_CS1#
- D[31..0] → D31..01
- CLK_OUT → CLK_OUT
- F_WE# → F_WE#

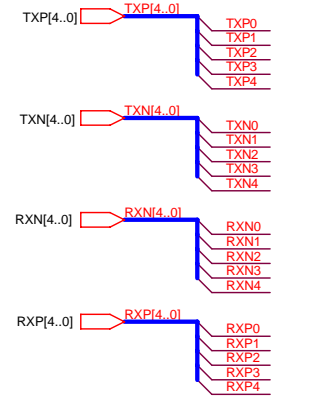
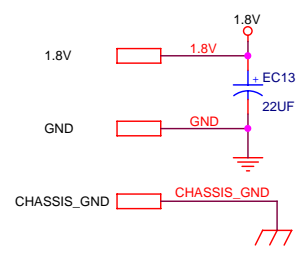


W986432DH (2Mx32)
SDRAM Bank 0

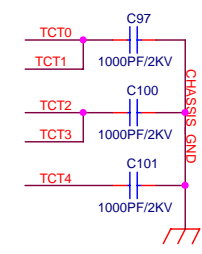
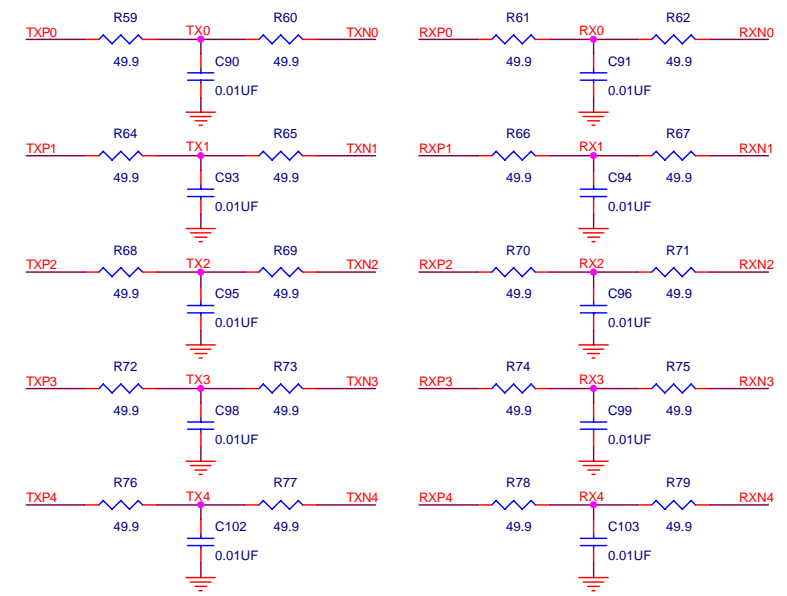
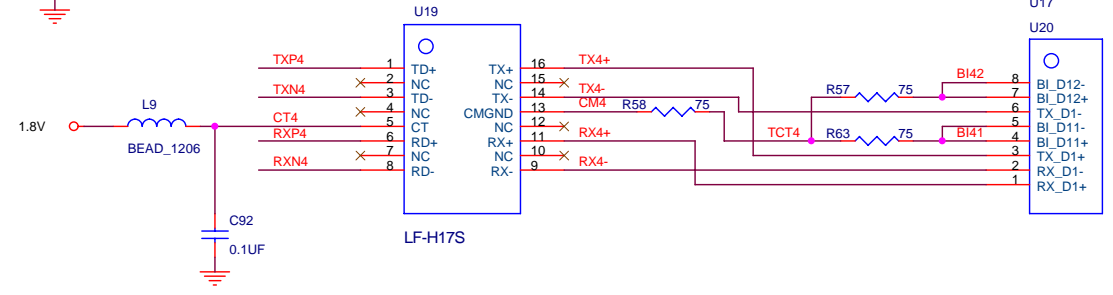
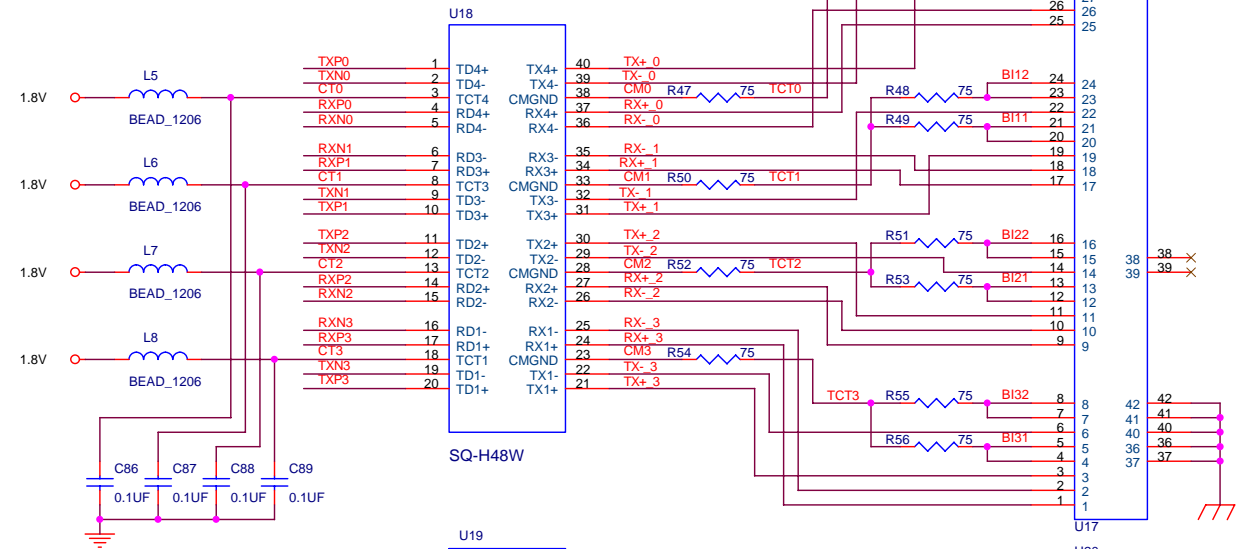


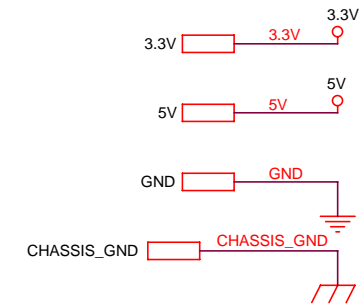
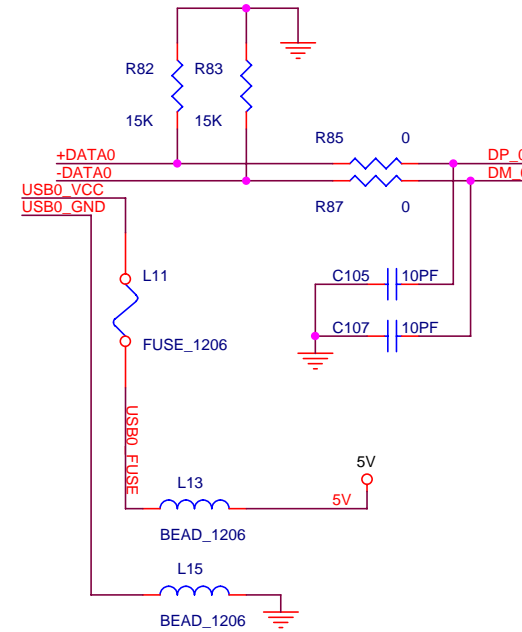
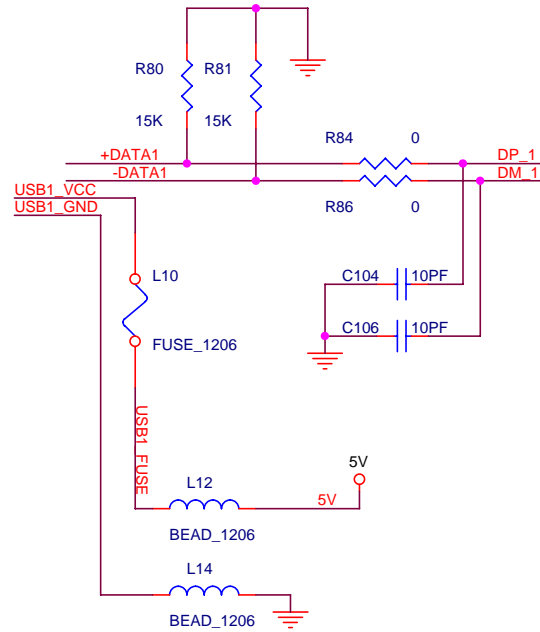
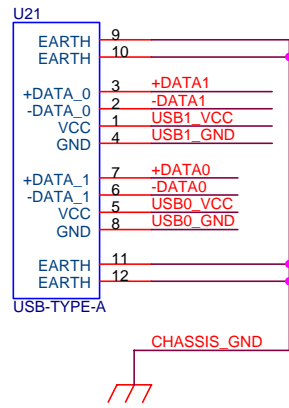
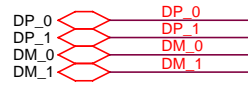
W986432DH (2Mx32)
SDRAM Bank 1

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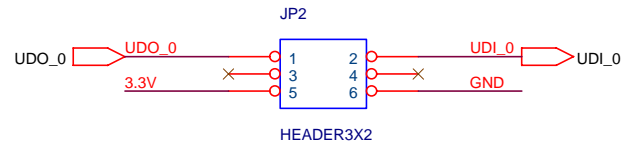


AUTO MDIX

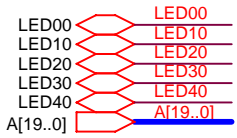
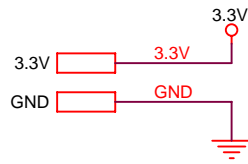




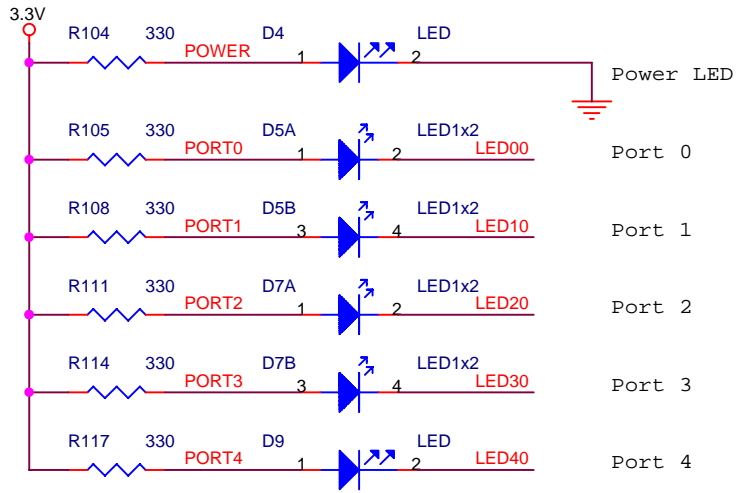
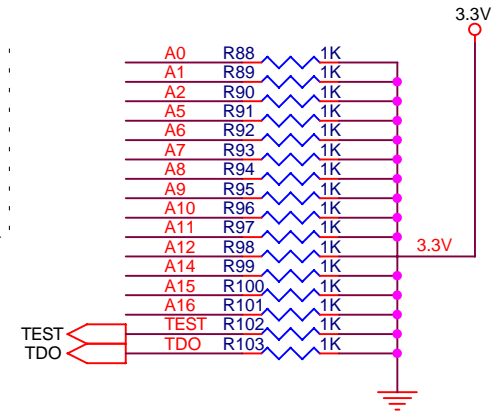
UART Connector



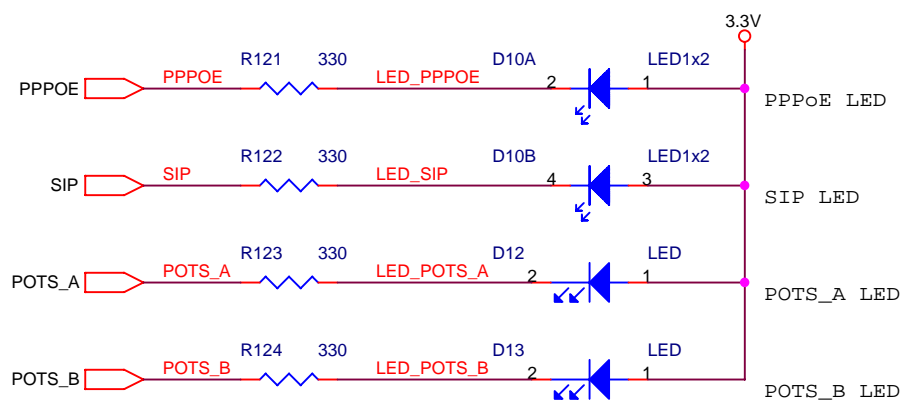
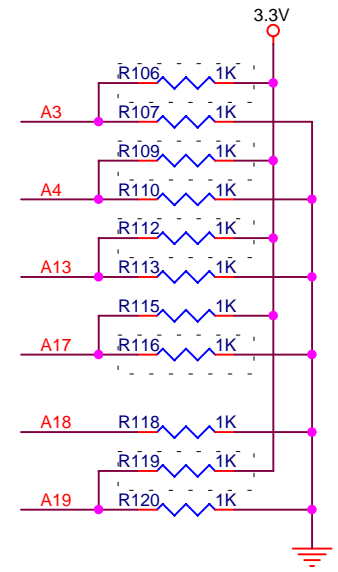
Infineon ADMtek		
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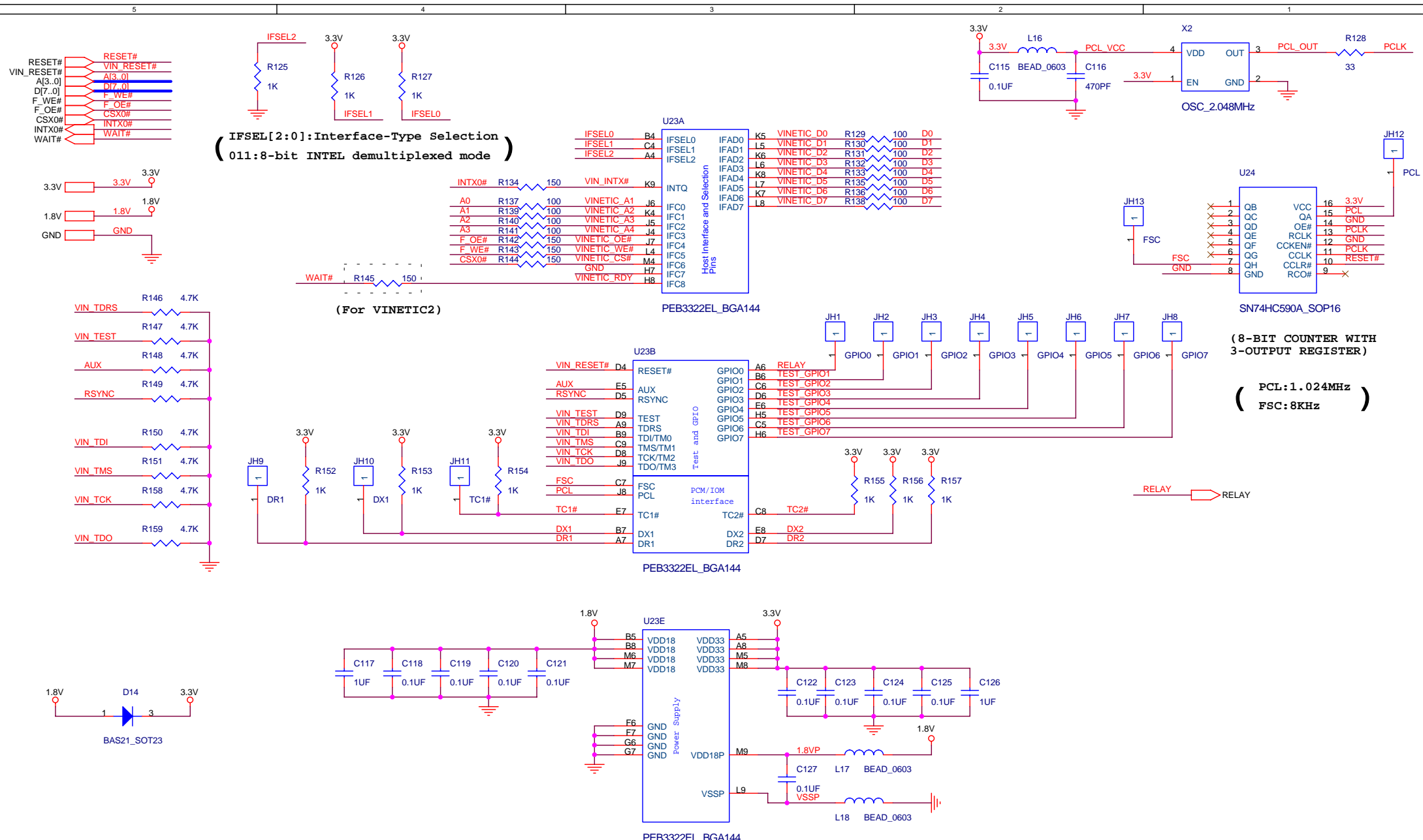
A1: NAND boot, pull down to disable
 A2: Auto MDIX, pull down to enable
 A12: Model, pull up to QFP package
 (for internal use)
 TEST, TDO: TEST mode,
 pull down for normal use.



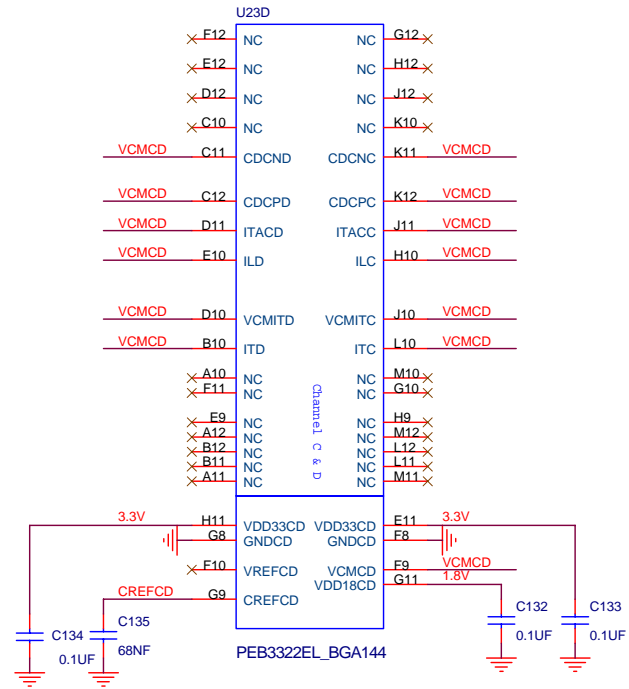
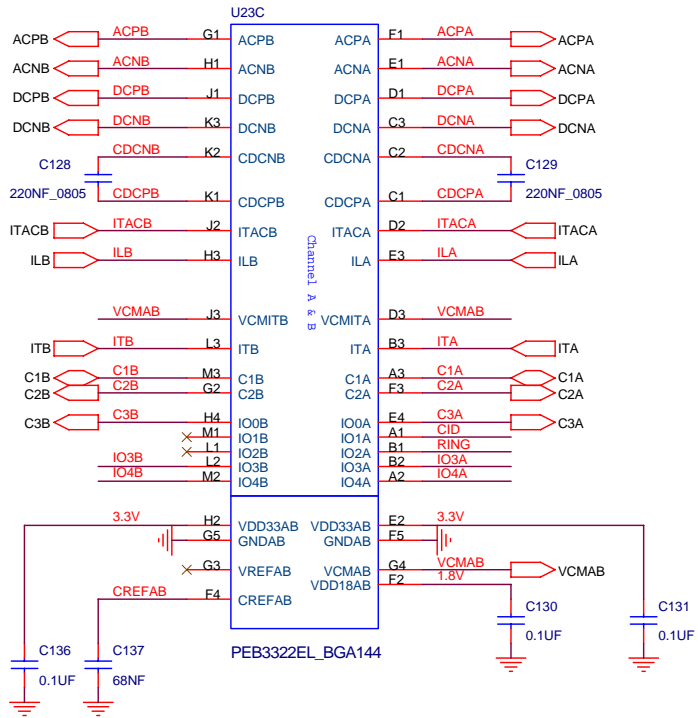
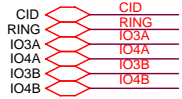
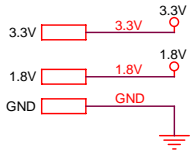
A4-A3: Pll setting
 00=175MHz (default)
 01=200MHz
 10,11=Reserved
 A13: Separate Power,
 0: PHY separate power on disable
 (default)
 1: PHY separate power on enable
 A18-A17: Nor flash boot
 00: boot in 8 bit.
 01: boot in 16 bit. (default)
 10,11: Reserved
 A19: endian
 0: little endian (default)
 1: big endian



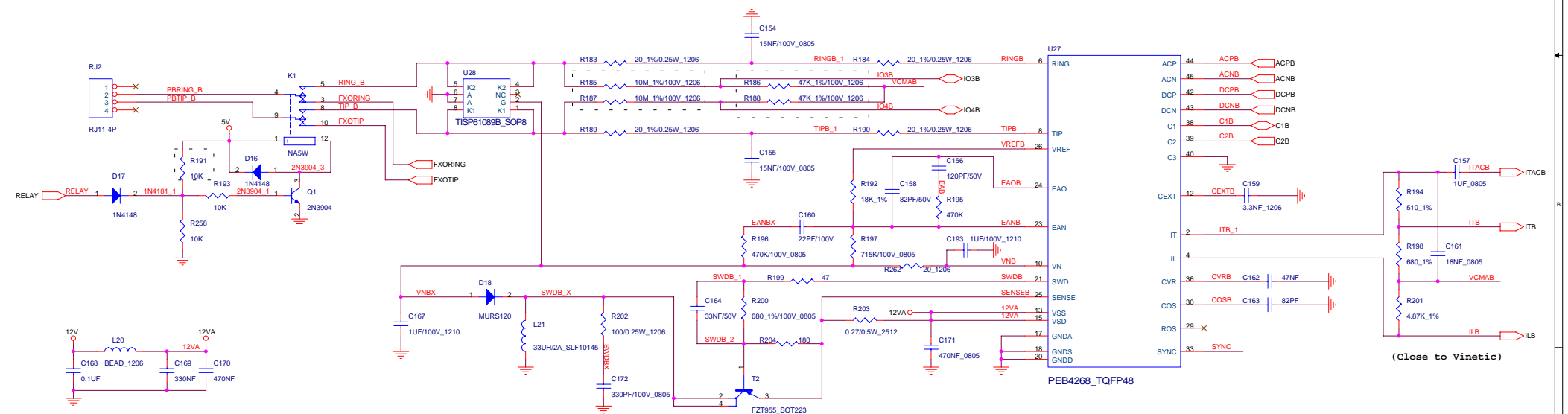
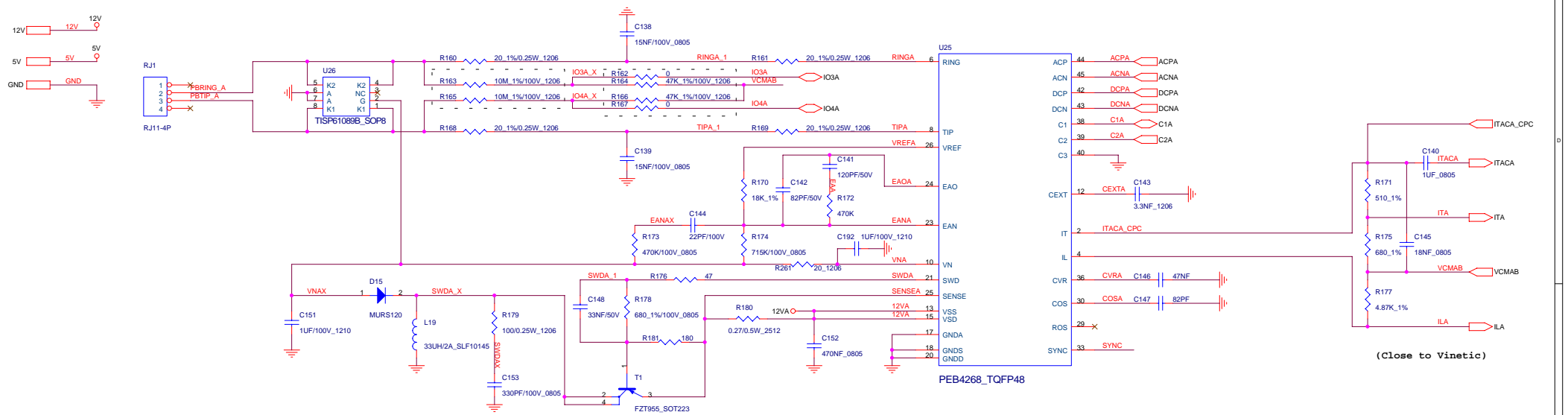
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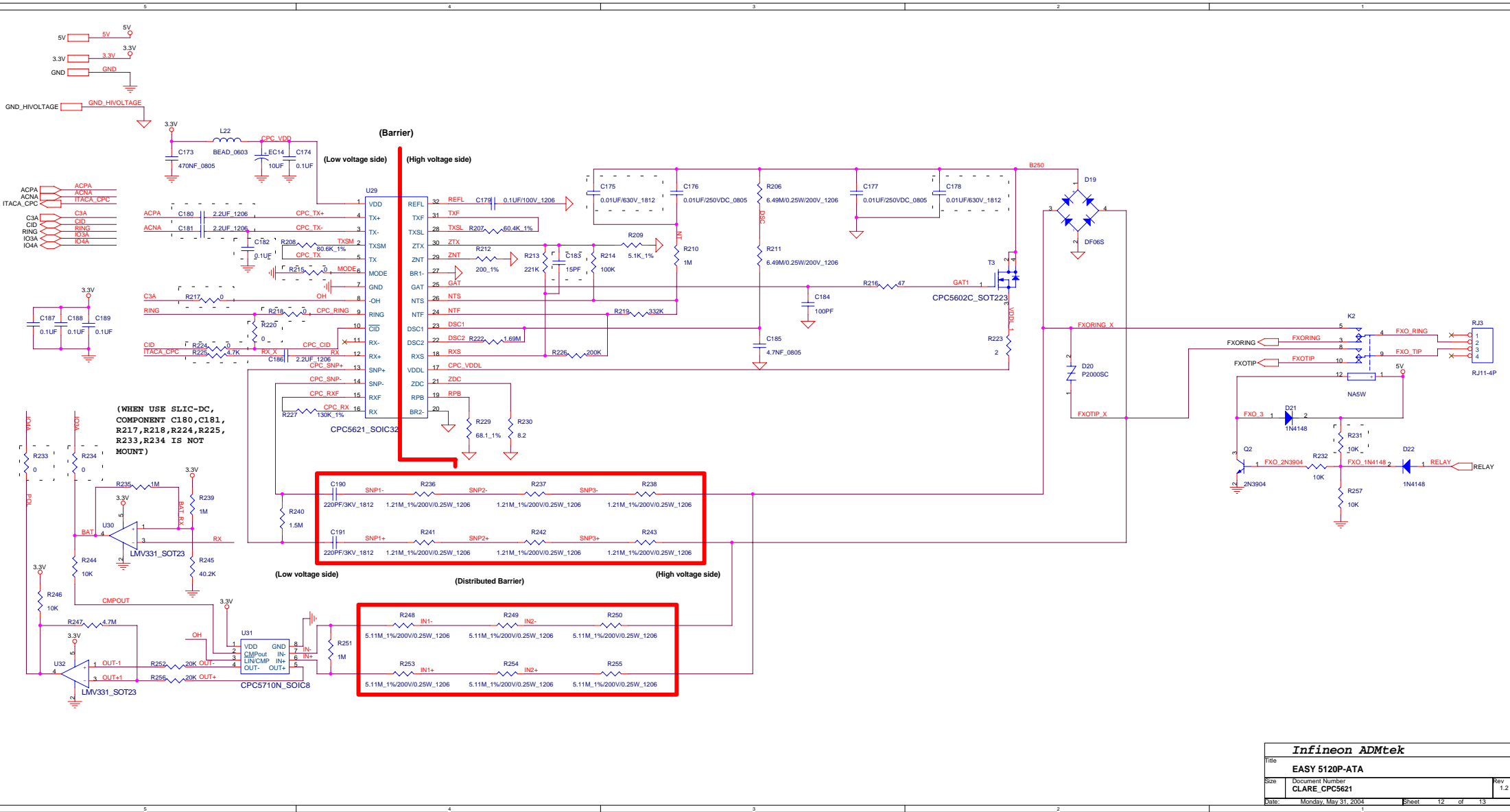


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Rev	Modification
1.0	- First draft
1.1	- SLIC-DC major change release state
1.2	<ul style="list-style-type: none"> - Change C151,C167 to 1uF/100V(TDK) - Change R/C filter (R261,C192 and R262,C193) position - Change R261,R262 footprint from 0603 to 1206 - Change pin40 of U25,U27 connection to GND - Change R177,R201 to 4.87K ohm - Change C192,C193 footprint from 1812 to 1210 - Change R196,R197,R200 footprint from 0603 to 0805 - Change R173,R174,R178 footprint from 0603 to 0805 - Change R180,R203 to 0.27 ohm

<i>Infineon ADMtek</i>		
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