ADM5120

HOME GATEWAY CONTROLLER

Product Notes

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About this Manual

Structure

This Data sheet contains 2 chapters

Chapter 1 Product Overview

Chapter 2 Packaging

Customer Support

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Chapter 1 Product Overview

1.1 Overview

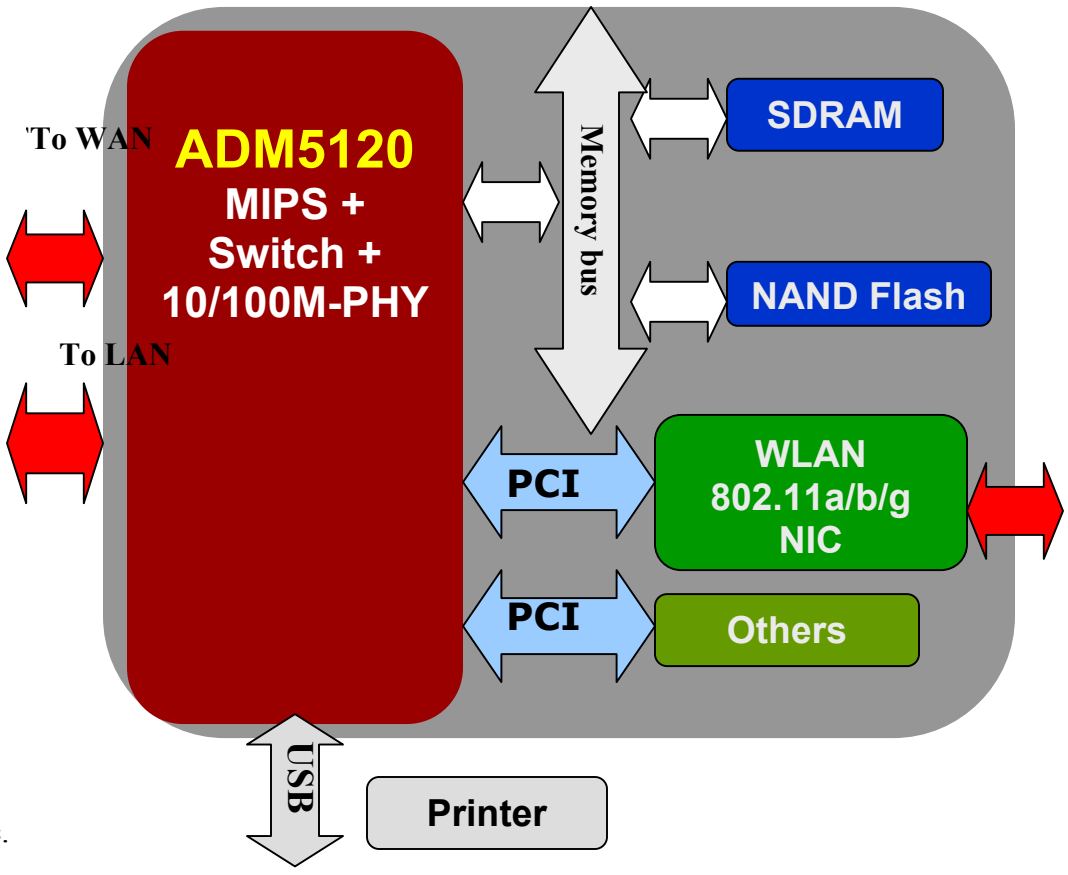
ADM5120 is a high performance, highly integrated, and highly flexible SOC (System-On-Chip) that facilitates the functionalities of SOHO/SME Gateway, NAT Router, Print Server, WLAN Access Point and VPN Gateway. ADM5120 enables the sharing of IP-based broadband services throughout the home/office using wired/wireless computers, entertainment equipment, printers, and other intelligent devices.

Internally, the ADM5120 ASIC consists of a high performance (227 MIPS) embedded MIPS CPU, an embedded switch engine, 10/100M PHY, an embedded PCI bridge, an embedded USB host, and interfaces for UART, SDRAM and Flash. The following diagram illustrates a system configuration that uses the supported functionalities/facilities of ADM5120.

1.1.1 Product Order Information

The ADM5120 comes in two packaging formats as follows:

Section 2.1 Ball Grid Array (BGA) 324-pin
Section 2.2 Plastic Quad Flat Pack (PQFP) 208-pin



1.2 Features

ASIC Features

Processor

- MIPS 4Kc CPU
- Embedded cache, 8K-byte I-cache, 8K D-cache
- Embedded memory management unit (MMU) – 32-entry TLB, organized as 16 entry pairs
- 175 MHz/227 MIPS

Network

- 6 ports
  - IEEE 802.3 Fast Ethernet
  - 5 auto-MDIX (auto-crossover) twisted paired LAN interfaces, embedded 10/100M PHY
  - 1 GMII(*)/MII interface
  - Flexible WAN port selection
- Embedded switch engine
  - Embedded Data-buffer/Address-look-up table
  - Look-up table read/write-able
  - MAC layer security
  - MAC clone solution
  - Multicast grouping (IGMP)
  - MAC filtering, Bandwidth control
- Class of Services (CoS) with two priority levels
- Shared dynamic data buffer management, embedded SSRAM
- Port grouping VLAN (overlap-able)
- TCP/IP accelerator

Memory interface

- SDRAM
  - Two bank support (2 chip select pins)
  - Each bank can support -- 1Mx32 up to 32Mx32bit (128M-byte)
- Flash
  - NAND Flash boot (*)
  - NOR Flash boot: Two bank support (2 chip select pins)
  - NOR Flash boot: Each bank can support – 1Mx8-bit, up to 1Mx32-bit (4M-byte)

System

- UART interface (support MODEM interface)
- PCI bridge that supports 3 master devices (*)
- GPIO (**)
- USB 1.1 host
- Clock source
  - 25MHz crystal for 10/100
  - 48MHz crystal for USB
- 0.18u CMOS process
- 1.8V/3.3V dual power
- BGA/PQFP

*** Available in BGA only, not PQFP**
**** PQFP has 4 GPIO pins v.s. BGA has 8 pins.**

Software Features

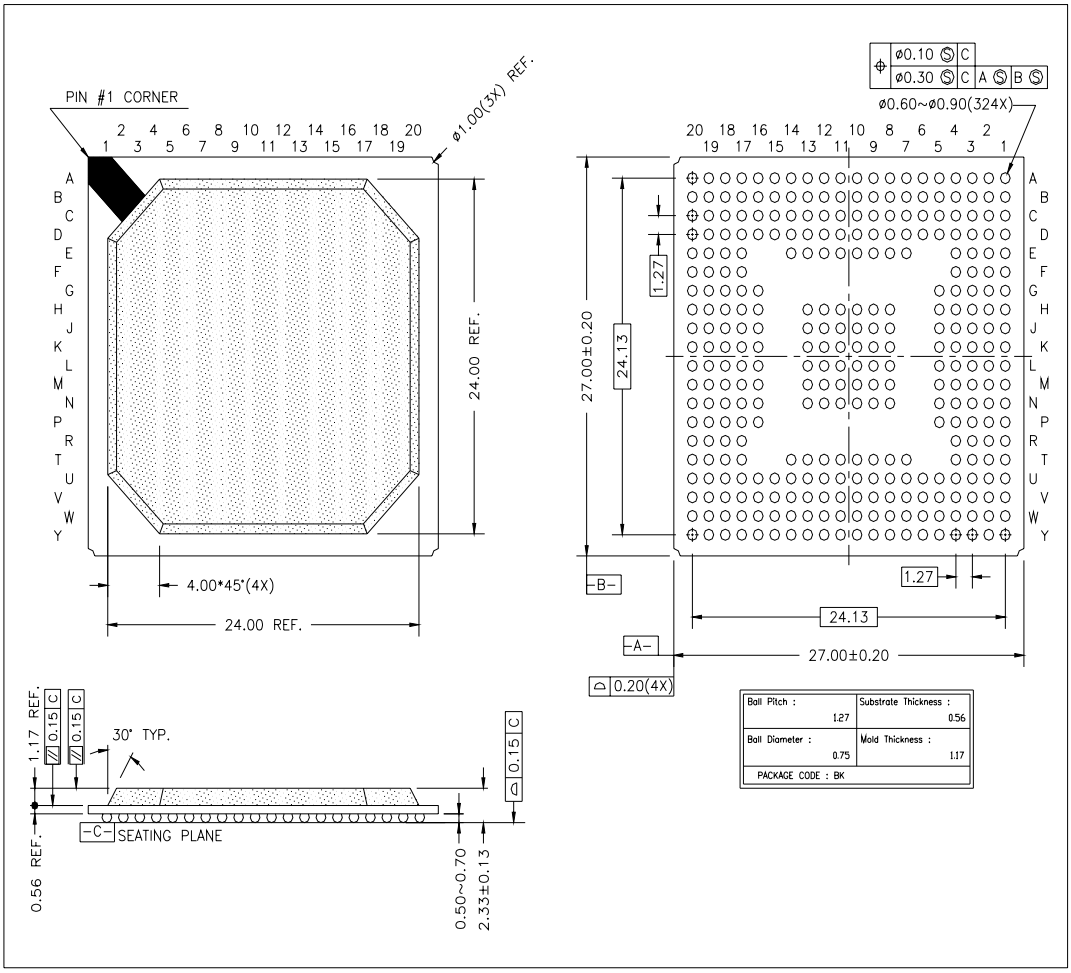
- Linux/Nucleus Real-Time OS
- Linux-based and Nucleus-based turn key support
- Telnet
- IEEE 802.3 Ethernet Driver
- IEEE 802.11 WLAN Driver
- RS232 Driver for Console User Interface
- DHCP Server/Client
- PPP over Ethernet (PPPoE)
- Network Address Translation (NAT) for IP Address Mapping/Sharing/Security
- DNS Proxy
- Simple Network Time Protocol (SNTP)
- Firewall
- Web-Based Configuration: WEB and HTTP
- TFTP upload/download

Typical Applications

- IEEE 802.3 SOHO/SME Gateway
- NAT Router
- Single band 802.11g Access Point (through PCI bus: 5120+802.11g NIC)
- Multiple band 802.11a/b/g Access Point (through PCI bus: 5120+802.11a/b/g NIC)
- Print Server (through USB1.1)
- 12-port SME Gateway (through GMII: 5120+6999U)

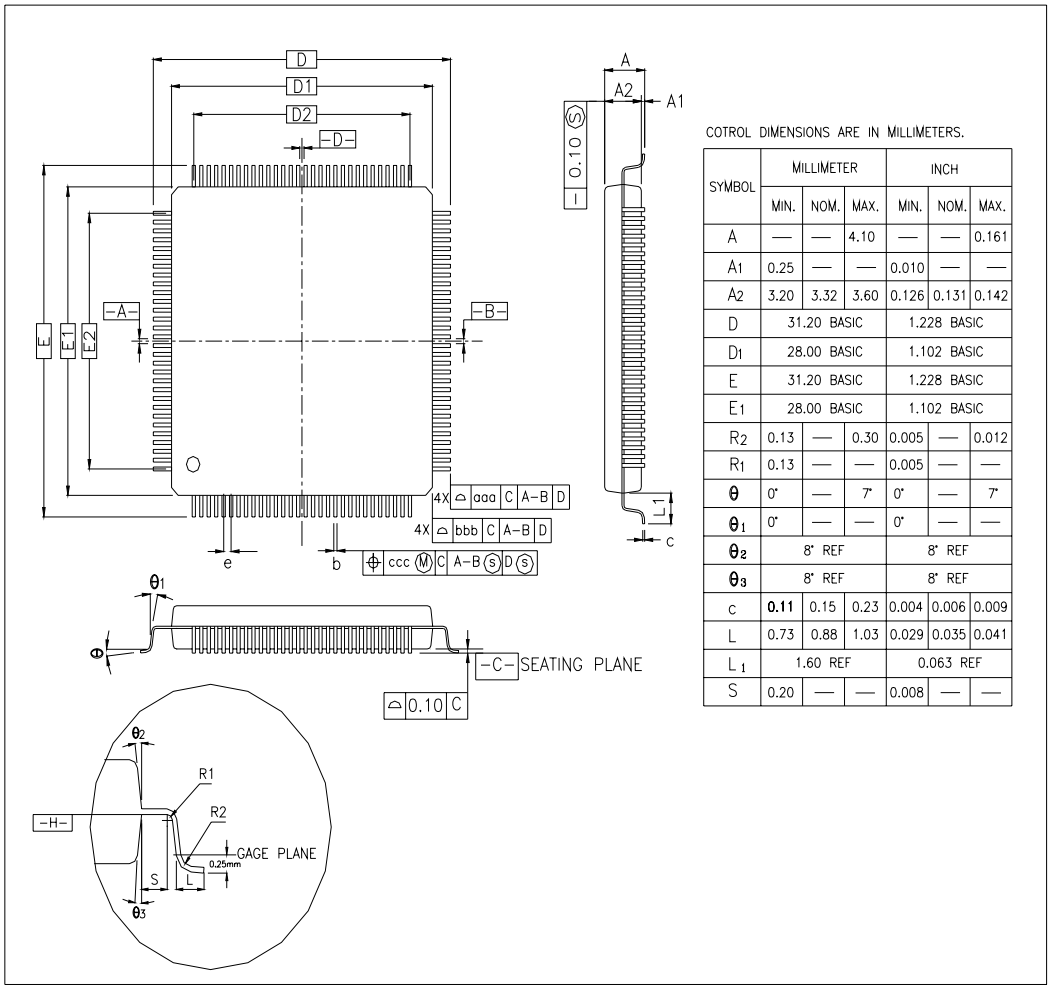
Chapter 2 Packaging

2.1 Ball Grid Array (BGA) 324-pin



Note: Scale = mm

2.2 Plastic Quad Flat Pack (PQFP) 208-pin



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D_1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E_1	28.00 BASIC			1.102 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

Note: Scale = mm

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		